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User Manual

Tektronix

VX4240
Waveform Digitizer/Analyzer Module

070-9140-06

This document supports firmware version 1.00 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

CE

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For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

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EC Declaration of Conformity

We

Tektronix Holland N.V.
Marktweg 73A
8444 AB Heerenveen
The Netherlands

declare under sole responsibility that the

VX4240 and Options 01 and 02 only

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility and Low Voltage Directive 73/23/ECC for Product Safety. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EMC Directive 89/336/EEC:

EN 55011 Class A Radiated and Conducted Emissions

EN 50081-1 Emissions:

EN 60555-2 AC Power Line Harmonic Emissions

EN 50082-1 Immunity:

IEC 801-2 Electrostatic Discharge Immunity
IEC 801-3 RF Electromagnetic Field Immunity
IEC 801-4 Electrical Fast Transient/Burst Immunity
IEC 801-5 Power Line Surge Immunity

Low Voltage Directive 73/23/EEC:

EN 61010-1/A2 1995 Safety requirements for electrical equipment for measurement, control, and laboratory use

To ensure compliance with EMC requirements this module must be installed in a mainframe that has backplane shields installed that comply with Rule B.7.45 of the VXIbus Specification. Only high quality shielded cables having a reliable, continuous outer shield (braid & foil) that has low impedance connections to shielded connector housings at both ends should be connected to this product.

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ERROR CODES

The error codes and error messages which may be returned by the VX4240 Module are as follows: (3 - 60)

00 NO ERRORS
01 LCA LOAD FAILURE
02 CPU RAM FAILURE (Uxxx) ADDR yyyyyyyy: OUT zz IN ww
03 COMMAND STRING EXCEEDS 160 BYTES
04 BOARD NOT CALIBRATED
05 INVALID COMMAND 'x'
06 NUMBER ABOVE MAXIMUM FOR 'x' COMMAND
07 NUMBER BELOW MINIMUM FOR 'x' COMMAND
08 THRESHOLD VALUE EXCEEDS THE VOLTAGE RANGE
09 COMMAND NOT IMPLEMENTED 'x'
10 IMPROPER COMMAND TERMINATION 'x'
11 RESERVED
12 (NUMBER OF RECORDS * RECORD SIZE) EXCEEDS MEMORY LIMIT
13 RESERVED
14 CONVERSION ERROR, NO NUMBER FOUND 'x'
15 CONVERSION ERROR, INVALID ARGUMENTS 'x'
16 CONVERSION ERROR, OUT OF RANGE 'x'
17 CALIBRATION ERROR, CANNOT ADJUST RANGE xxx OFFSET
18 CALIBRATION ERROR, CANNOT ADJUST RANGE xxx GAIN
19 OFFSET FAILURE - RANGE xxx (VALUE y.yyyyyyyE+yyy)
20 GAIN FAILURE - RANGE xxx (VALUE y.yyyyyyyE+yyy)
21 NON-VOLATILE MEMORY FAILURE (Uxxx) OUTyyyy IN zzzz
22 HIGH SPEED RAM FAILURE (BANK xxx) ADDR yyyyyyyy: OUT zzzz IN wwww
23 RESERVED
24 ADDRESS READBACK FAILURE (U02/U22) OUT xxxxxxxx IN yyyyyyyy
25 ADDRESS COUNTER FAILURE (Uxxx) OUT yyyyyyyy IN zzzzzzzz
26 THRESHOLD COMPARATOR FAILURE (Uxxx) OUT yyyyyyyy IN zzzzzzzz
27 DATA EXTENSION FAILURE (U431/U631) OUT yyyyyyyy IN zzzzzzzz
28 RESERVED
29 RECORD MODE READBACK FAILURE (U42/U71) OUT yyyy IN zzzz
30 POSITIVE INPUT FAILURE (U120/K1201) (VALUE = y.yyyyyyyyE+yyy)
31 NEGATIVE INPUT FAILURE (K1401) (VALUE = y.yyyyyyyE+yyy)
32 DIFFERENTIAL (CMRR) INPUT ERROR (VALUE = y.yyyyyyyE+yyy)
33 AC COUPLING FAILURE (K1501): (VALUE = y.yyyyyyyE+yyy)
34 SAMPLE COUNTER FAILURE (Uxxx) COUNT yyyy SAMPLES zzzz
35 RESERVED
36 MEASUREMENT COMPLETE STATUS BIT NOT ACTIVE (Uxxx)
37 ARMED STATUS BIT NOT ACTIVE (Uxxx)
38 TRIGGERED STATUS BIT NOT ACTIVE (Uxxx)
39 DONE STATUS BIT NOT ACTIVE (Uxxx)

VX4240 Waveform Digitizer/Analyzer Module QUICK REFERENCE GUIDE

Numbers in parentheses refer to the page(s) in the Operating Manual.

SETUP

Be sure all switches are correctly set. (p. 1 - 4)
Follow Installation guidelines. (p. 2 - 1)

The default condition of the VX4240 Module after the power-up self test is:
Mode: software trigger
Collect: Post-trigger; count = RAMsize - 100 (RAMsize = amount of memory on board)
Level 1: +100
Level 2: -100
Voltage: ±100V, dc coupled, 1 MOhm input impedance, single-ended BNC input
Frequency: 10 MHz, internal clock
Delay: 0
All interrupts disabled
All control I/O signals negative edge triggered
VXI output trigger disabled
Real time update frequency: 10 MHz
Block delimiter: semi-colon

LEDs

When lit, the LEDs indicate the following:

POWER	power supplies functioning
SYSFAIL	module failure
MSG	module is processing a VMEbus cycle
RFI	indicates a Request True interrupt is pending on the backplane
BINARY	Binary Transfer mode is in effect
GATE	gate input is active
CLOCK	flashes at the frequency of the sample clock
ARM	the module is "armed" and awaiting or processing the trigger
DIFF	the module is in the Differential Input mode
TRG	the module's trigger has occurred
Z50	input load is 50 Ohms
MIP	indicates that sampling is taking place
AC	the input signal is ac coupled
MC	conversion process is complete
CIN	signal input is being taken from the DB25 connector

Front Panel Display - shows "BUSY" when a command is being processed, then "RDY" or "E-xx", where xx is the error number.

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SYSTEM COMMANDS

These VXIbus Instrument Protocol commands are initiated by the VX4240's commander, and will affect the module:

ABORT NORMAL OPERATION
ASYNCHRONOUS MODE CONTROL
BEGIN NORMAL OPERATION
BYTE AVAILABLE
BYTE REQUEST
CLEAR
CONTROL EVENT
END NORMAL OPERATION
ERROR QUERY
IDENTIFY COMMANDER
READ PROTOCOL
READ STATUS
TRIGGER

COMMAND SYNTAX

Command protocol and syntax for the VX4240 is as follows: (3 - 4)

1) A command string is a string of up to 160 valid ASCII characters (p. 3 - 5) terminated by a <LF>. Enter multiple commands in a string by using a semi-colon as a delimiter between individual commands.

2) Valid command delimiters are <LF> and (;).

3) If any invalid characters are received, they are ignored.

4) Commands can be issued at any time.

5) If errors occur, the error number will be displayed. All commands will be ignored until either the E or R command is issued.

6) A character not enclosed by brackets is sent a shown, otherwise:
[] encloses the symbol for the actual argument to be sent.
<CR> carriage-return. <SP> space character.
<LF> line-feed. <TM> terminator: <LF> or ;

7) Any character may be sent in either upper or lower case form.

8) Numeric values: fixed or floating-point formats; no embedded spaces; all numbers rounded to the nearest value. If no sign is specified, the number is assumed to be a positive value.

MODULE COMMANDS

To begin operation, use the set-up commands to define the operating parameters:

B generates an interrupt to the system controller on a programmed condition. (3 - 53)
C specifies the data collection mode. (3 - 55)
D specifies the time delay between the trigger event and when data collection begins. (3 - 59)
F specifies the sampling frequency. (3 - 63)
I sets up the format and addresses of data read from the VX4240's memory. (3 - 65)
L defines the delimiting character between data values. (3 - 72)
M specifies the trigger condition for which data collection begins. (3 - 73)
P specifies the sampling period. (3 - 63)
T arms the trigger. (3 - 84)
V specifies voltage range, input coupling, input load, and input type. (3 - 89)
W specifies the active edges of the control signals. (3 - 91)

When set-up is complete, use the T command to begin sampling.

A The Analyze commands execute pre-programmed routines to analyze the sampled data (3 - 7). Figure 4 (3 - 52) shows the responses graphically. The command set consists of 23 two-letter commands, where the second letter specifies what is to be analyzed:

A	Average value (3 - 10)	F	Fall time (3 - 21)
B	Ringing high (3 - 11)	G	Record operations (3 - 23)
C	Fast Fourier transform (3 - 13)	H	FFT w/Hanning compress. (3 - 25)
D	Difference (3 - 18)	I	Integrate (3 - 26)
E	Ringing low (3 - 19)	K	Peak-to-peak voltage (3 - 27)
M	Minimum value (3 - 31)		
N	Maximum negative transition (3 - 32)	T	True rms value (3 - 41)
O	Overshoot (3 - 33)	U	Undershoot (3 - 42)
P	Maximum positive transition (3 - 35)	V	Pulse parameters (3 - 44)
Q	FFT/Blackman-Harris (3 - 36)	W	Pulse width (3 - 42)
R	Rise time (3 - 37)	X	Maximum value (3 - 48)
S	Statistics (3 - 39)	Y	Cycle count (3 - 49)
Z	Zero crossing times (3 - 50)		

J allows the module to perform arithmetic operations. (3 - 68)
L Single frequency discrete Fourier transform (DFT) (3 - 29)

The set of status commands report information about the system, the module, or the current operation:

E used to examine error conditions. (3 - 60)
G reports the greatest or least value seen since the last trigger. (3 - 64)
K calculates the gain and offset for a specified voltage range. (3 - 70)
O returns the programmed operational setup parameters of the VX4240 to be activated by the T command. (3 - 76)
R returns the VX4240 Module to its default, power-up state. (3 - 81)
S causes the module to execute a self test. (3 - 82)
U allows reading the current record number, "in-progress" data, or loading the real time update count. (3 - 88)
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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

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WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

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Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

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VX4240

Waveform Digitizer/Analyzer Module

Section 1
General Information and Specifications

Introduction

The VX4240 Waveform Digitizer/Analyzer Module is a printed circuit board assembly for use in a C or D size mainframe conforming to the VXIbus Specification. It combines a 12-bit, 10 MHz, A/D (analog-to-digital) converter with a state-of-the-art RISC transputer to provide a very sophisticated measurement and analysis tool. Capable of capturing waveforms in the dc to 5 MHz frequency range, the VX4240 features extensive, on-card signal analysis and conditioning routines. All key parameters are programmable, and calibration is greatly simplified by semi-automatic calibration alignment software.

In addition to collecting and transferring waveforms, the VX4240 can analyze and/or preprocess sample data before returning it to the system controller. The more than 40 signal analysis routines available include such functions as fast Fourier transforms (FFT) using any of three different windows; signal to noise ratio; total harmonic distortion; maximum, minimum, average, and RMS values; rise and fall times; pulse widths, peak-to-peak voltages; overshoot and undershoot; mean and standard deviation; and period, frequency, and duty cycle.

Another unique feature of the VX4240 is its ability to directly set the desired input range. Eight of the ranges (0.5, 1, 2, 5, 10, 20, 50, and 100 Volts) are calibrated, but any range of less than 100 Volts may be set. If a range other than a calibrated range is selected, the VX4240 will pre-scale the signal using a Tek-developed virtual ranging circuit. This circuit, in effect, adjusts the incoming signal so that 12-bit weighting is provided at any voltage within the VX4240's range, allowing it to outperform many 14-bit digitizers. The input can be programmed to be ac- or dc-coupled and single ended or differential, with either 50 Ohms or 1 MOhm input impedance.

Besides triggering commands that support pre-triggered, center-triggered, post-triggered, or free running data collection, a Record mode is available which automatically rearms the trigger each time a programmed number of samples has been taken. Any of the analysis routines can be performed on any record or records. Trigger sources may be external, on command, the VXI backplane, the VXI command trigger, or either or both of two independently programmable threshold triggers. Any two AND or OR combinations of these triggers can be set for more precise trigger control.

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A programmable time delay will delay data collection after a trigger for from 200 nsec to 420 sec. The sample clock is programmable from 0.005 Hz to 10 MHz and can be referenced to an internal clock, an external clock, or the VXIbus 10 MHz ECL clock.

Other features include nonvolatile memory for storage of calibration parameters; external arm, trigger, clock, and gate inputs; trigger, clock, and armed outputs; multiple interrupt conditions; "in-progress" reading of the input voltage; and extensive status information displayed by LEDs on the front panel.

Accessories

Standard Accessories included with the VX4240.

VX1742P	**Data Cable**
VX1782P	**Data Cable**

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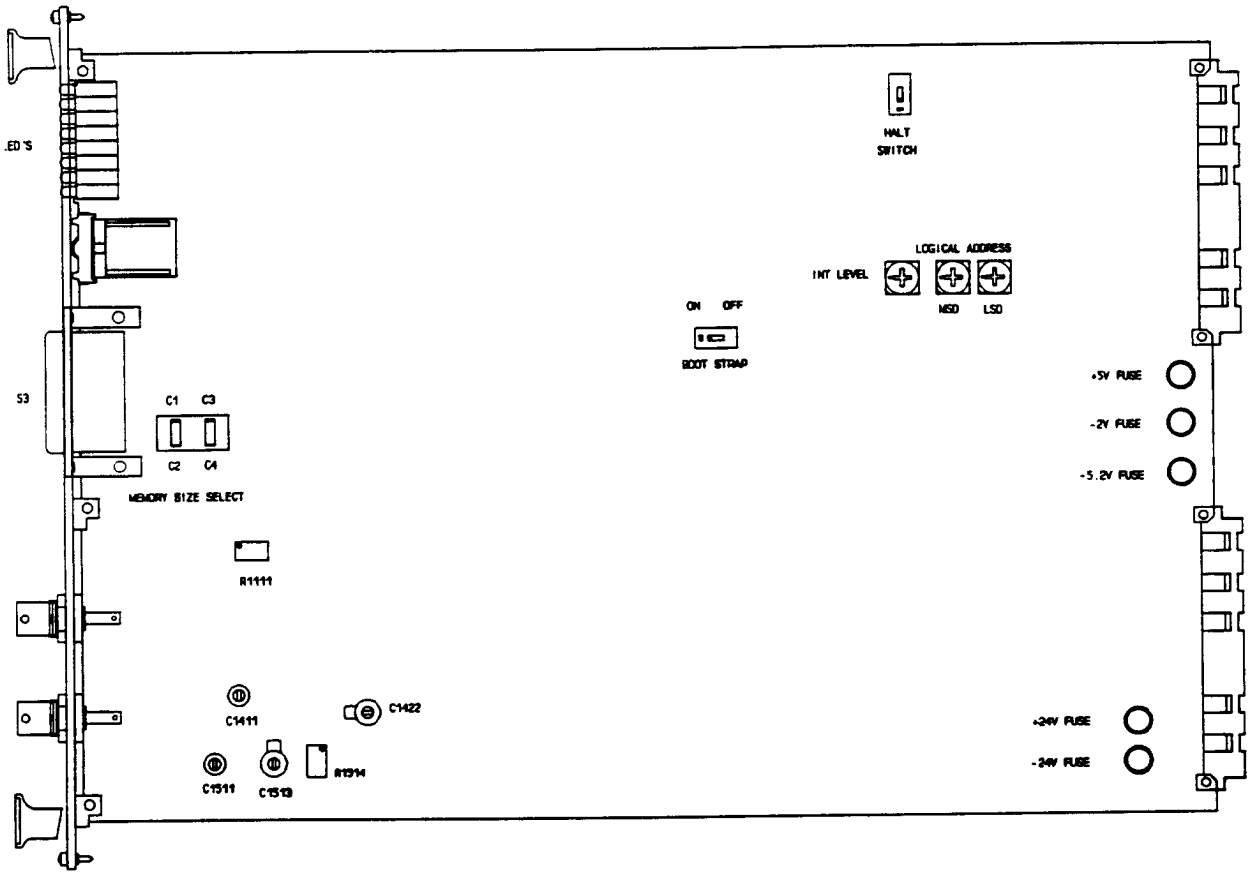

Figure 1: VX4240 Controls and Indicators

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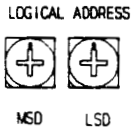
Controls And Indicators

The following controls and indicators are provided to select and display the functions of the VX4240 Module's operating environment. See Figure 1 for their physical locations.

Switches

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4240 is set to a value between 1 and FEh (257d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield. If the switchs are set to FFh (255d), the VX4240 becomes dynamically configured. Refer to the resource manager manual to determine what will occur at system configuration.

The actual physical address of the VX4240 Module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4240 will be [(64d * XYh) + 49152d]. For example:

L.A.	MSD	LSD	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the VX4240 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address. Refer to *Appendix K: IEEE-488 Address* if you are using a National Instruments GPIB-VXI/C Slot 0 module.
If the VX4240 is being used with a Tektronix/CDS IEEE-488 interface module, consult the operating manual of the Tektronix/CDS Resource Manager/IEEE-488 Interface Module being used.

If the VX4240 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC). This algorithm is described in detail in the 73A-156 Operating Manual.

If the VX4240 is not being used with a Tektronix/CDS Resource Manager/IEEE-488 Interface Module, consult the operating manual of the IEEE-488 interface device being used for recommendations on setting the logical address.

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INT LEVEL

VMEbus Interrupt Level Select Switch

Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander. When using the VX4240 with a Tektronix/CDS commander module, set the interrupt level to the same level as the interrupt handler on that commander. The VMEbus interrupt level on which the VX4240 Module generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the VX4240's interrupt handler, typically the module's commander. Setting the switch to an invalid interrupt level (0, 8, or 9) will disable the module's interrupts.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

HALT SWITCH

Halt Switch (S084)

This two-position slide switch selects the response of the VX4240 Module when the Reset bit in the module's VXIbus Control register is set.

This switch must be set ON. If the Halt switch is in the OFF position, this instrument will not operate correctly.

If the Halt switch is in the OFF position, the module will ignore the Reset bit and no action will take place. Note that the module is not in strict compliance with the VXIbus Specification when the Halt switch is OFF. Control of the Reset bit depends on the capabilities of the VX4240's commander.

Bootstrap Switch (S56)

This two-position slide switch is only used for factory testing, and must be set to the OFF position.

Memory Size Switch (S80)

This switch is factory set to specify the amount of memory present on the module. The settings are:

S80		Words of Memory
C1	C4	256K
C2	C4	512K
C2	C3	1M

LEDs

The following LEDs are visible at the top of the VX4240 Module's front panel to indicate the status of the module's operation.

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POWER LED
This LED is normally lit and is extinguished if the ±5V, -2V, or ±24V power supplies fail, or if the ±5V, -2V, or ±24V fuses blow.

SYSFAIL LED
This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete a self test, loss of a power rail, or failure of the module's central processor.

If the module loses any of its power voltages, the Failed LED will be lit and SYSFAIL* asserted. A module power failure is indicated when the module's Power LED is extinguished.

MSG LED (Message)
This LED is normally off. When lit, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a five microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

RFI (Request for Interrupt)
When lit, this LED indicates a Request True interrupt is pending on the backplane. It is cleared when the interrupt is serviced.

BINARY
When lit, this LED indicates the Binary Transfer mode is in effect. Refer to ***Appendix J: Binary Transfer*** if you are using a National Instruments GPIB Slot 0 module.
GATE (Gate Hold)
When lit, this LED indicates that the gate input is active.

CLOCK (Sample Clock)
This LED flashes at the frequency of the sample clock. For sample rates faster than approximately 30 Hz, the LED appears to be lit continuously.

ARM (Armed)
When lit, this LED indicates that the module is "armed" and awaiting or processing the trigger. This LED goes out when data sampling is complete.

DIFF (Differential Input)
When lit, this LED indicates the module is in the Differential Input mode.

TRG (Triggered)
When lit, this LED indicates that the module's trigger has occurred.

Z50 (50 Ohm Input)
When lit, this LED indicates the input load is 50 Ohms.

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MIP (Measurement In Progress)
This LED indicates that sampling is taking place. The LED is turned off whenever the memory is full, the memory is accessed, the trigger is rearmed in the Record mode, or the VX4240 Module is halted or reset (see Operation section).

AC (AC Coupled)
When lit, this LED indicates the input signal is ac coupled.

MC (Measurement Complete)
When lit, this LED indicates that the conversion process is complete. This occurs whenever the memory is full, the memory is accessed, or the module is halted or reset.

CIN (Connector In)
When lit, this LED indicates the signal input is being taken from the DB25 connector (S3).

Front Panel

A four character display on the front panel provides information on current operation. Whenever a command is being processed, the character display will show "BUSY". On completion, the display will show "RDY" or "E-xx", where xx is the error number.

The front panel has two BNC inputs labeled SIG IN+ and SIG IN-, and one DB25S connector labeled S3. Refer to Appendix B for connector pinouts.

Fuses

The VX4240 Module has +5V, -5.2, -2V, +24V, and -24V fuses. The fuses protect the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

If any fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

If any fuse opens, remove the fault before replacing the fuse. Replacement fuse information is given in the Specifications section of this manual.

BITE (Built in Test Equipment)

Built in Test Equipment (BITE) is provided by extensive self tests that are automatically performed on power-up and may also be invoked on command. Circuitry tested includes the CPU and all memory; A to D's; thresholds, latches and counters; and the analog front end, including the signal path (using an internal voltage reference), common mode, coupling, offset, and range gain. A series of LEDs provide visual BITE for sampling, clock, measurement cycle, source, gate activity, arming and trigger conditions, interrupts, and input mode, source, impedance, and coupling. A four element pixel display on the front panel provides information on operation and error conditions.

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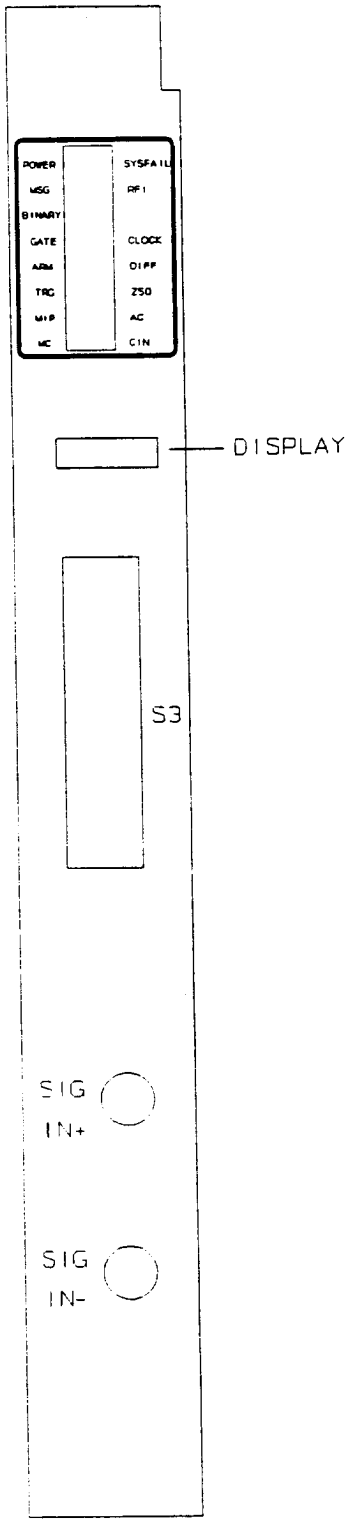

Figure 2: VX4240 Front Panel

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Specifications

* indicates programmability

***Input Voltage Ranges:** ±0.5, ±1.0, ±2.0, ±5.0, ±10.0, ±20.0, ±50.0, and ±100.0 Volts (calibrated range values). A continuous ("virtual") ranging capability is provided.

***Sampling Frequencies:** 0.005 Hz to 10 MHz.

***Sample Intervals:** 100 ns to 200 s (internal and VXI clocks) in 100 ns steps. External clock (100 ns minimum period).

Signal Input:

***Type:** Differential, single-ended.

Bandwidth: dc to 5 MHz (-3 dB ±1 dB at 5 MHz).

Roll-off: -6 dB/octave (5-10 MHz).
-18 dB/octave (10-20 MHz).

***Coupling:** ac, dc, ground.

***Impedance:** 50 Ohm ±1%, < 20 pF.
1 Megohm ±3%, < 20 pF.
929 Kohm ±2% < 20 pF (50V and 100V ranges).

CMRR: > 40 dB (dc to 1 KHz) (100:1).
> 50 dB (316:1) 50 Ohm typical.
> 60 dB (1000:1) 1 Mohm typical.

Resolution (for twelve bits):

Range (V)	Resolution (mV/b)
±100	48.828
±50	24.414
±20.0	9.7656
±10.0	4.8828
±5.0	2.4414
±2.0	0.97656
±1.0	0.48828
±0.5	0.24414

Accuracy: DC accuracy error (using average function):
< 0.2% of full scale ('full scale' is delta between maximum and minimum value in a range; for example, 2V in the ±1V range)
< 0.4%, ±0.5V range.
Temperature drift: <0.03% of full scale /°C (all ranges)

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Dynamic Accuracy: based on least squares fit to idealized 12-bit sine wave and the formula:

Effective bits = 12 - [$\log_2$ (RMS error actual/RMS error ideal)]

Effective Bits/Typical

Range	10 KHz	100 KHz	1 MHz
0.5	> 9.36	> 9.28	> 8.14
1 V	> 9.51	> 9.44	> 8.13
2 V	> 9.00	> 8.89	> 8.15
5 V	> 9.49	> 9.01	> 7.98
10V	> 9.28	> 8.4	> 7.75
20V	> 8.6	> 7.62	--
50V	> 9.5	> 9.21	--
100V	> 28.87	> 8.42	--

Sample Memory:

Depth: 256K words (options for 512K and 1Mword).

*Control:
Pre-trigger.
Center-trigger.
Post-trigger.
Free-running.
Record mode.

*Triggering:
± External TTL-edge.
Dual ± Voltage thresholds.
Automatic (on command).
VXI TTL trigger (1 of 8 programmable).
VXI command trigger.
Any AND/OR combinations of the above.

External Trigger Uncertainty: ≤ 1 sample clock period (Trigger to first sample).

Trigger Rearm Time: 1 sample clock period (Record mode).

*Voltage Threshold Trigger Range: ±0 to ±100% full scale.

Voltage Threshold Resolution: 8 bits.

Sample Clock Accuracy: 5 ppm/yr.

External Sample Clock: TTL level, 1 50 Ohm load; dc to 10 MHz.

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Delay Times:	External clock rising edge to sample delay: 30 ns ±10 ns. Sample clock to clock out delay: 12 ns ±5 ns.
*Delayed Triggering Range:	200 ns to 420 s (in 200-ns increments).
Delay Uncertainty:	≤ 200 ns (delay time). ≤ 1 sample clock (delay sample).
Gate Uncertainty:	≤ 1 sample clock (gate transition to sampling).
Data Output:	
*Formats:	ASCII. Binary. Two's-complement binary. ASCII blocks (DMA).
*Memory Control:	± offset from trigger. Auto-increment. Auto-decrement.
Processor:	
CPU:	INMOS T800 floating point transputer.
Memory:	128K bytes RAM, 128K bytes EPROM.
Embedded Preprocessor Software Routines:	Maximum value. Minimum value. Maximum value since trigger. Minimum value since trigger. Maximum positive transition. Maximum negative transition. Average value. RMS value. Ringing. Integrate. Difference. Peak-to-peak. Pulse width. Rise time. Fall time. Distortion (overshoot/undershoot). Fast Fourier Transform (FFT). Signal to noise ratio. Total harmonic distortion. Signal to noise and distortion.

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Spurious free dynamic range.
Mean/standard deviation.
Period.
Frequency.
Duty cycle.

I/O Connections:

2 - BNC Jacks.
1 - DB25 25 pin connector.

Inputs:

TRIG IN, one TTL load, programmable to positive or negative edge true.

CLK IN, 50 Ohm load.
Clock high time minimum: 50 ns.
Clock low time minimum: 50 ns.

ARM IN, one TTL load programmable to positive or negative edge true.

GATE, one TTL load, active low.
Gate high time minimum: 50 ns.
Gate low time minimum: 50 ns.

SIG IN + (BNC): CAT II, 150 V DC, 120 V AC, into 1 M Ohm 10 V DC, 50 Ohms

SIG IN – (BNC): CAT II, 150 V DC, 120 V AC, into 1 M Ohm 10 V DC, 50 Ohms

Outputs (TTL):

CLK OUT, TTL, 50% duty cycle, 50 Ohm line driver.

TRIG OUT, TTL, programmable to active low or high (trigger detection).

ARM OUT, TTL, programmable to active low or high.

Self Test:

The module automatically performs a self test on power-up. The test consists of verifying the CPU and data memory, module's internal buses, and analog input circuitry. Self test may also be performed on command.

VXIbus Compatibility:

Fully compatible with the VXIbus Specification V1.4 for message-based instruments with the Halt switch in the ON position.

VXI Device Type:

VXI message based instrument.

VXI Protocol:

Word serial.

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Dynamic Configuration:	Yes (set LA switch to FFh).
VXI Card Size:	C size, one slot wide.
Module-Specific Commands:	All module-specific commands and data are sent via the VXIbus Byte Available command. All module-specific commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.
VMEbus Interface:	Data transfer bus (DTB) slave - A16, D16 only.
Interrupt Level:	Switch selectable, levels 1 (highest priority) through 7 (lowest); or programmable.
Interrupt Acknowledge:	D16; lower 8 bits returned are the logical address of the module.
VXIbus Commands Supported:	All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command error: ABORT NORMAL OPERATION ASSIGN INTERRUPT LINE ASYNCHRONOUS MODE CONTROL BEGIN NORMAL OPERATION BYTE AVAILABLE (with or without END bit set) BYTE REQUEST CLEAR CLEAR LOCK CONTROL EVENT END NORMAL OPERATION ERROR QUERY READ INTERRUPT LINE READ INTERRUPTER READ PROTOCOL READ STATUS SET LOCK TRIGGER
VXIbus Protocol Events Supported:	VXIbus events are returned via VME interrupts. The following event is supported and returned to the module's commander: REQUEST TRUE (In IEEE-488 systems, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.)

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VXIbus Registers:	ID Device Type Status Control Protocol Response Data Low See Appendix A for definition of register contents.
Device Type Register Contents:	FDF7
Power Requirements:	All required dc power is provided by the Power Supply in the VXIbus mainframe.
Voltage:	+5 Volt Supply: 4.75 V dc to 5.25 V dc. -2 Volt Supply: -1.9V dc to -2.1 V dc. +24 Volt Supply: +23.5 V dc to +24.5 V dc. -24 Volt Supply: -23.5 V dc to -24.5 V dc.
Current (Peak Module, I_{PM}):	+5 Volt supply: 3.85A -5.2 Volt Supply: 0.6A -2.0 Volt Supply: 0.026 A +24 Volt Supply: 0.22 A -24 Volt Supply: 0.23 A
Fuses:	Replacement fuses: **Littelfuse** P/N 273005 (5 amp) and 273002 (2 amp) **125 V VFBIo (very fast blow).**
Cooling:	Provided by the fan in the VXIbus mainframe. Less than 10°C temperature rise with 2.7 liters/sec of air at a pressure drop of 0.19 mm of H_2O.
Temperature:	-10°C to +65°C, operating (assumes ambient temperature of 55° and airflow to assure less than 10°C temperature rise). -40°C to +85°C, storage.
Humidity:	Less than 95% R.H. non-condensing, -10°C to +30°C. Less than 75% R.H. non-condensing, +31°C to +40°C. Less than 45% R.H. non-condensing, +41°C to +55°C.
Radiated Emissions:	Complies with VXIbus Specification.
Conducted Emissions:	Complies with VXIbus Specification.
Module Envelope Dimensions:	197 mm high, 221 mm deep, 13 mm wide. (7.75 in x 8.69 in x 0.5 in).

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Dimensions, Shipping:	When ordered with a Tek/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, the module's shipping dimensions are: 254 mm x 254 mm x 127 mm. (10 in x 10 in x 5 in).
Weight:	Fully configured, with Option 02 and Option 03: 1.6 kg. (3 lb 8.4 oz.)
Weight, Shipping:	When ordered with a Tek/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1-12). When ordered alone, the module's shipping weight is: 2.1 kg. (4 lb 8.4 oz.)
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)
Front Panel Signal Connectors:	2 BNC inputs, 1 DB25S connector. Refer to Appendix B for connector pinouts.
Equipment Supplied:	1 - VX4240 Waveform Digitizer/Analyzer Module. 1 - Spare fuse +5V 1 - Spare Fuse, ±24V, -2V, -5.2V
Optional Equipment:	1 - 73A-742P 5-meter, 25 pin cable, unterminated.
Options:	01 512K memory. 02 1 Meg memory. 03 Digital Signal Processor.

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Conditions for Safety Certification:

Operating Temperature:	**+5 to +40 °C**
Maximum Operating Altitude:	**2000 m**
Equipment Type:	**Test and measuring**
Safety Class:	**Class I (as defined in in IEC1010-1, Annex H) grounded product.**
Overvoltage Category:	**Supply Input:** **Overvoltage Category I (as defined in IEC1010-1, Annex J).** **Measuring Inputs:** **Overvoltage Category II (as defined in IEC1010-1, Annex J).**
Pollution Degree:	**Pollution Degree 2 (as defined in IEC1010-1). Rated for indoor use only.**

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Section 2
Preparation For Use

Installation Requirements And Cautions

The VX4240 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus mainframe slot other than slot 0. If the module is being installed in a D size mainframe, consult the operating manual for the mainframe to determine how to install the module in that particular mainframe. Setting the module's Logical Address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the VX4240 Module's logical address. To avoid confusion, it is recommended that the slot number and the logical address be the same.

Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

WARNING. *To avoid electric shock, tighten the module mounting screws after installing the module into the mainframe to ensure that the front panel is properly grounded.*

NOTE. *There are two labeled printed ejector handles on the card. To install the card correctly, make sure the ejector labeled "VX4240" is at the top. In order to maintain proper mainframe cooling, unused mainframe slots must be covered with the blank front panels supplied with the mainframe.*

NOTE. *Verify that the mainframe is able to provide adequate cooling and power with this module installed. Refer to the mainframe Operating Manual for instructions.*

Based on the number of IAC modules ordered with a Tek/CDS mainframe, blank front panels are supplied to cover all unused slots. Additional VXIbus C size single-slot and C size double-slot blank front panels can be ordered from your Tektronix supplier.

CAUTION

Verify that the mainframe is able to provide adequate cooling and power for the VX4240 Module. Refer to the mainframe Operating Manual for instructions on determining cooling and power compatibility.

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If the VX4240 is used in a VX1X Series Mainframe, all VX4240 cooling requirements will be met.

CAUTION

If the VX4240 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the VX4240 Module to operate properly. Check the manual of the mainframe being used for jumpering instructions.

If a Tek/CDS VX1400 or VX1401 mainframe is being used, the jumper points may be reached through the front of the mainframe. There are five (5) jumpers that must be installed for each empty slot. The five jumpers are the pins to the left of the empty slot.

Installation Procedure

CAUTION

The VX4240 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the module's Revision Level, Serial Number (located on the label on the top shield of the VX4240), and switch settings on the Installation Checklist. Only qualified personnel should install the VX4240 Module.

2) Verify that the switches are switched to the correct values. DO NOT adjust the factory settings on the Bootstrap switch or the Memory Size switch.

   The Halt switch should be in the ON position unless it is desired to not allow the resource manager to reset this module. Note that with either Halt switch position, a "hard" reset will occur at power-on and when SYSRST* is set true on the VXIbus backplane. If the module's commander is a VX4520 Slot 0 Device/Resource Manager, SYSRST* will be set true whenever the Reset switch on the front panel of the VX4520 is depressed. Also note that when the Halt switch is in the OFF position, the module is not in strict compliance with the VXIbus Specification.

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3) The module can now be inserted into any slot of the chassis other than slot 0.

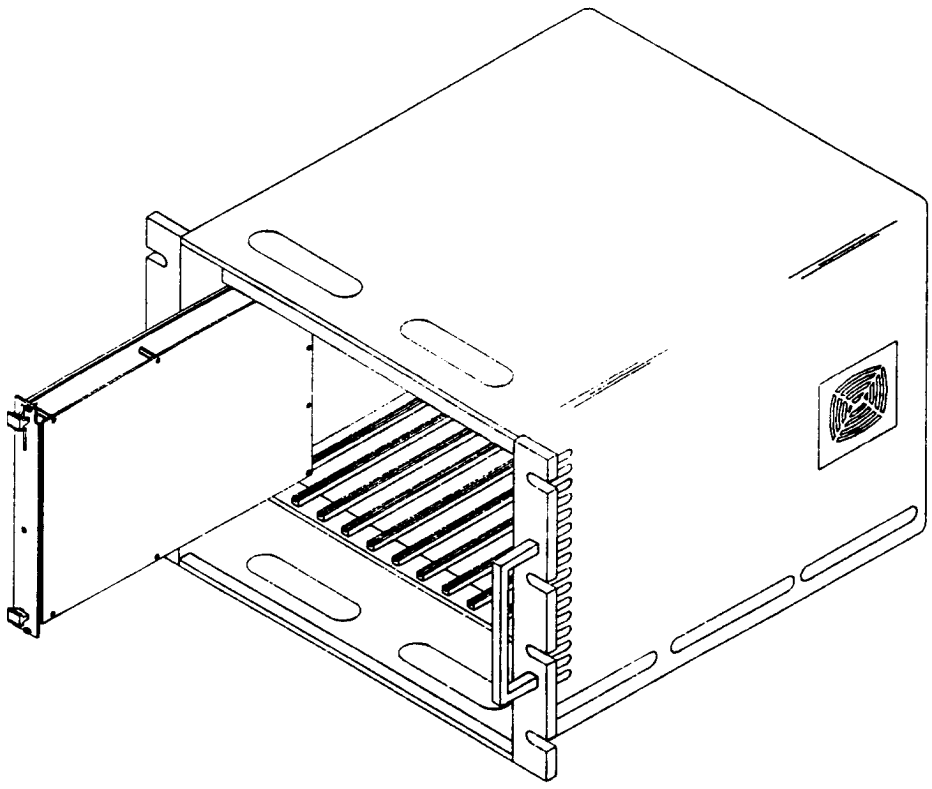

Figure 3: Module Installation

4) **Installation of Cables -**
Use an RG58 Coax Cable to interface between the module BNC connector(s) and the Unit Under Test (UUT). If the mainframe has a cable tray, route the cable from the front panel of the module down through the cable tray at the bottom of the mainframe and out the rear of the mainframe.

If a special cable is needed, a CDS 73A-742P Hooded Connector may be used to cable between the module's DB25 connector and the UUT.

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Installation Checklist

Installation parameters may vary depending on the mainframe being used. Be sure to consult the mainframe Operating Manual before installing and operating the VX4240 Module.

Revision Level: _____

Serial No.: _____

Mainframe Slot Number: _____

Switch Settings:

VXIbus Logical Address Switch: _____ (FFh enables dynamic configuration.)

Interrupt Level Switch: _____

Halt Switch: must be set ON for correct operation

Memory Size Switch: (Factory Setting)

S80: C1 __
C2 __
C3 __
C4 __

Bootstrap Switch: __OFF__

Cable Hooded Connector Installed: (if any)

RG58 Coax Cable: __

73A-742P Hooded Connector: __

Performed by: _____ Date: _____

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Section 3
Operation

Overview

In addition to the primary capability of capturing waveforms ranging in frequency from dc to 5 MHz, the module also incorporates extensive waveform analysis routines and includes many programmable features.

The sample clock can be programmed to select either the internal clock (programmable from 0.005 Hz to 10 MHz), an external clock, or the VXIbus 10 MHz ECL clock.

Input voltage ranges can be set from ±0.5 Volts to ±100 Volts, including any non-standard range values. Signal inputs can be ac or dc coupled, single ended or differential, and loaded with 50 Ohms or 1 MOhm.

The triggering commands that control waveform acquisition support pre-triggering, center-triggering, post-triggering, or free running (trigger-independent) data collection. A Record mode is also supplied which automatically rearms the trigger each time a programmed number of samples has been taken. Trigger sources are external, internal (on command), the VXI backplane trigger, VXI command trigger, or two independently programmed threshold triggers. Any two AND or OR combinations of these triggers can be set for precise trigger control. A time delay is also provided to delay data collection after a trigger. The delay can be programmed from 200 nsec to 420 sec.

The standard VX4240 Module has 256 K words of memory, and options can increase this to 1 Mword.

Data can be rapidly sent from the Waveform Digitizer/Analyzer to the system controller in binary, two's complement binary, ASCII, or ASCII blocks, starting at any point in memory relative to the trigger point.

In addition to collecting and transferring waveforms, the VX4240 Module contains embedded software routines. These routines allow preprocessing the stored data before returning it to the system controller. Preprocess signal analysis routines are available for such functions as maximum, minimum, average, and rms values; rise and fall times; pulse widths, peak-to-peak voltages; overshoots and undershoots; mean and standard deviation; period, frequency, and duty cycle; fast Fourier transforms (FFT); signal to noise ratio; and total harmonic distortion.

Other features include nonvolatile memory for storage of calibration parameters; external arm and gate inputs; trigger, clock, and armed outputs; multiple interrupt conditions; "in-progress" reading of the input voltage; and extensive status information available from the module and displayed on the front panel.

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The module is a VXIbus Message Based instrument and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the VX4240 Module's commander for details on the operation of that device.

If the module is being used in a TEK/CDS VX7401 System mainframe, the module's commander will be a Slot 0 Device/Resource Manager. Refer to the commander's Operating Manual and the programming examples in the Operation section of this manual for information on how the system controller communicates with the VX4520.

Start-up

The VX4240 Module will complete its self test and be ready for programming five seconds after power-up. The VXIbus Resource Manager may add an additional one or two second delay. The Power LED will be on. The MSG LED will blink during the power-up sequence as the VXIbus Resource Manager addresses all modules in the mainframe. The default condition of the module after power-up is described in the SYSFAIL, Self Test and Initialization subsection.

Whenever a command is being processed, the front panel display will show "BUSY". On completion, the display will show "RDY" or "E-xx", where xx is the error number.

The VX4240 Module is programmed by ASCII characters issued from the system controller to the VX4240 Module via the module's VXIbus commander and the VXIbus mainframe backplane. The format and syntax for the command strings is described in the Module Command sub-section. An alphabetical listing of the complete description of each command is in the Command Descriptions sub-section. A sample BASIC program using these commands is shown in the Programming Examples section.

To begin operation, use the set-up commands to define the operating parameters:

B Backplane Interrupt - generates an interrupt to the system controller on a programmed condition.

C Collect - specifies the data collection mode (pre-trigger, center-trigger, post-trigger, free-run, Record mode).

D Delay - specifies the time delay between the trigger event and when data collection begins.

F Frequency - specifies the sampling frequency.

I Input - sets up the format and addresses of data read from the VX4240 Module's memory.

L Define Delimiter - defines the delimiting character between data values, where large blocks of data are being transferred.

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M Trigger Mode - specifies the trigger condition for which data collection begins.

P Period - specifies the sampling period.

T Trigger - arms the trigger.

V Voltage - specifies the voltage range (as a continuous parameter), input coupling, input load, and input type.

W Control Signal Edges - specifies the active edges of the control signals.

When set-up is complete and the module is correctly programmed, use the T (Trigger) command to begin sampling.

The A (Analyze) commands execute pre-programmed routines to analyze the sampled data. The J (Math Operations) command allows the VX4240 to be used as a calculator to perform arithmetic operation, which may be required for data analysis.

The set of status commands report information about the system, the module, or the current operation:

E Error - used to examine error conditions.

G Greatest Value - reports the greatest or least value seen since the last trigger.

K Calibrate - calculates the gain and offset for a specified voltage range.

O Operational Setup - returns the operational setup parameters of the VX4240 Module.

Q Query - returns module status information.

R Reset - returns the VX4240 Module to its default, power-up state.

S Self Test - causes the module to execute a self test.

U Update - allows reading the current record number, "in-progress" data, or loading the real time update count.

Z Version Level - returns the card number and the current software version level.

System Commands

Although these non-data commands are initiated by the VX4240's commander (for example, the VX4520 Module) rather than the system controller, they have an effect on the VX4240 Module. The following VXIbus Instrument Protocol Commands will affect the VX4240:

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Command	Effect
Clear	The module clears its VXIbus interface and any pending commands. Current module operations are unaffected.
Trigger	If programmed, this command is used to trigger the VX4240 sampling process.
Begin Normal Operation	The module will begin operation if it has not already done so.
Read Protocol	The module will return its protocol to its commander.
Read Status	The module will return its status to its commander.

Module Commands

Syntax

Command protocol and syntax for the VX4240 Module are as follows:

1) A command string consists of a string of ASCII encoded characters (up to 160 maximum) terminated by a <LF>. Multiple commands may be entered within a string, with a semi-colon used as a delimiter between individual commands.

2) Valid command delimiters for the VX4240 Module are the line-feed <LF>, and the semicolon (;). The command string is buffered up until a <LF> is encountered, at which time the entire string is evaluated. For example, "F10E6;VI;CT;T<LF>" is a valid command string.

   If no delimiter is entered, then the card interprets the next command as being part of the previous command. This causes either an error or an improper setup.

3) The set of valid ASCII characters for the VX4240 Module is given below. If any other characters are received, they are ignored.

4) Commands can be issued at any time. If the Frequency, Period, Voltage, Trigger Mode, Collect Mode, or Delay command is issued while the card is collecting data, the command will be queued and executed when the next trigger command is received. After one of these commands is received, it remains valid until it is respecified or until the card is reset.

   An Input, Analyze, or Greatest Value command will terminate collection of data. A Query or Operational Setup command is executed immediately, does not terminate collection, and will give the present status at any time.

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5) If any commands are improperly loaded, the error number will be shown on the front panel display. The invalid command and all subsequent commands will be ignored until either the Error command is issued (see the E command), or the card is reset (see the R command).

If input from the card is requested while an error is queued, the card's status (see the Q command) will be returned instead of the requested data.

6) If a character is not enclosed by brackets, that character itself is sent, otherwise:

[] encloses the symbol for the actual argument to be sent. These argument symbols are defined under each command heading.

<CR> carriage-return.

<LF> line-feed.

<SP> space character.

<TM> terminator: indicates a line-feed or semicolon.

7) Any character may be sent in either upper or lower case form.

In the command descriptions, "RAMsize" refers to the amount of sample memory on the board.

Numeric Value Formats

When specifying numeric values, fixed or floating-point formats are allowed. No embedded spaces are allowed. All numbers are rounded to the nearest value appropriate for the particular command (rounded down if exactly half way), except where otherwise noted in the text. If no sign is specified, the number is assumed to be a positive value.

A number whose absolute value is 5 can be represented by any of the following:

5	+.5E1
+05	+50E-1
5.0	0.0000000000000005E+16
0.5E+01	

Valid ASCII Characters

The valid ASCII characters for the VX4240 Module are as follows:

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Character(s)	Hexadecimal Equivalent
A through Z	41 through 5A
a through z	61 through 7A
0 through 9	30 through 39
&	26
#	23
+	2B
-	2D
.	2E
/	2F
;	3B
<LF>	0A

Any character other than the above is treated as white space (is ignored), and is allowed anywhere except in a numeric value. Any number of white space characters may be used together.

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Command Descriptions In the following descriptions, "RAMsize" refers to the amount of sample memory on the board.

Command: A (Analyze)

Syntax: A[z]

Purpose: The Analyze command executes preprogrammed routines for analysis of the stored information.

Description: The Analyze command set consists of 23 two-letter commands, where the second letter, [z], specifies what is to be analyzed. [z] can be any one of the following:

[z]	Definition
A	Average value
B	Ringing high
C	Fast Fourier transform (FFT)
D	Difference
E	Ringing low
F	Fall time
G	Record Operations
H	FFT with Hanning compression
I	Integrate
K	Peak-to-peak voltage
L	Single frequency discrete Fourier transform (DFT)
M	Minimum value
N	Maximum negative transition
O	Overshoot
P	Maximum positive transition
Q	FFT with Blackman-Harris window
R	Rise time
S	Statistics (mean, standard deviation)
T	True rms value
U	Undershoot
W	Pulse width, periods, duty cycles
X	Maximum value
Y	Cycle count
Z	Zero crossing times, periods, duty cycles

Each of these commands is described in detail in the following pages. This discussion applies to the set of all A commands.

If the A command permits or requires an [x] and/or [y] argument following the command, that argument is defined as follows (unless specified otherwise):

[x] Optional count from 1 to RAMsize, specifying the number of samples. If [x] is not specified, it defaults to RAMsize.

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[y] Optional starting address from -RAMsize to +RAMsize. If y is not specified, it defaults to the address of the oldest data in memory. For example, if CP100 were programmed, the oldest data is at location 100, and is the default starting address. CT100 has the oldest data at location −100. CC has the oldest data at -RAMsize/2. The trigger address is address 0.

If the module has been programmed in the Record mode, the A command can be executed on individual records. The syntax is:

AzR[n]/[x]/[y]

where [n] is the record number (from 1 to the total number of records). [x] and [y] are as defined above, except that [y] defaults to the starting address of the record.

When using the waveform analysis commands, the signal should be oversampled by a minimum of 10, with an amplitude greater than ±5% of the programmed range. That is, the sampling frequency should be a minimum of 10 times the input signal frequency. The greater the oversampling and/or the greater the amplitude, the more accurate are the results. This applies to the AB, AE, AF, AK, AO, AR, AU, AW, and AZ commands.

If a response value is followed by a number in parenthesis, that number is the memory location of the response value, relative to the trigger (location 0). For records, that number is the address relative to the start of the record.

An underscore (_) in any example of a command response represents an ASCII space character (20 hex).

All numerical responses to the A commands are of the format ±x.xxxxxxxE±xxx where x is a decimal digit 0 through 9.

Figure 3 (at the end of the A command set, page 3 - 50) illustrates how the data is interpreted and gives a graphic example of the measurements taken for many of the A commands. Input requests immediately following an A command return the appropriate information. The 0% and 100% points are determined by a complex algorithm that establishes a "steady state" maximum or minimum level or slope, and uses the maximum or minimum (respectively) of that steady state term as the 100% and 0% points. In a perfect sine, square, or triangular wave, the 100% and 0% points will be equal to these maximum and minimum values.

To provide the capability to de-multiplex data, a step option has been provided for selected Analyze commands (software revision levels 1.5 and later). This option performs the requested analysis on the data at regularly spaced intervals. It is intended primarily for use with a multiplexer connected to the VX4240. The commands affected are the average value (AA), difference (AD), integrate (AI), minimum value (AM), maximum negative transition (AN), maximum positive

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transition (AP), statistics (AS), true RMS voltage (AT), and the maximum value (AX).

As an example, suppose the multiplexer was programmed to scan channels 0 through 3 in sequence. The multiplexer data for each of the four channels would be stored every fourth memory location in the VX4240's memory. Assuming synchronization between the triggers of the two cards, channel 0's data would be at addresses 0, 4, 8...; channel 1's at 1, 5, 9... etc.

You would use the command 'AX/0S4' to determine the maximum value of channel 0. This causes the card to search for the maximum value every fourth memory location, beginning at address 0 (the trigger address), for (RAMsize / 4) data values. The value returned would be the maximum value of channel 0 stored in the VX4240's memory. Similarly, for channel 1, the command 'AX/1S4' would begin the check every fourth location, beginning at address 1.

If a data count is given in the command, the memory is scanned for that many values. For example, 'AX1000/0S4' would scan every fourth memory location beginning at address 0, and ending at address 3999 (1000 data values = 4000 memory locations).

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Command: AA (Average value)

Syntax:
AA[x]/[y][Sz]
AAR[n]/[x]/[y][Sz]

Purpose: This command calculates the average value of the data in memory.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the size of the record, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

Examples:

AA/0	calculates the average value of RAMsize samples beginning at address 0 (the trigger address).
AA	calculates the average value of RAMsize samples beginning at the address of the oldest data in memory.
AA100	calculates the average value of 100 samples beginning at the address of the oldest data in memory.
AA100/3200	calculates the average value of 100 samples beginning at address 3200.
AAR3	calculates the average value of record 3.
AAR7/100	calculates the average value of the first 100 samples of record 7.
AAR1/100/200	calculates the average value of 100 samples of record 1 beginning 200 locations from the start of the record.
AA/0S4	calculates the average value of RAMsize/4 samples, for every fourth memory location, beginning at address 0.

Response Syntax: Average value of data in memory

AV=_+4.8828125E-002<CR><LF>

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Command: AB Ringing (high)

Syntax:
AB[H][x]/[y]
AB[H]R[n]/[x]/[y]

Purpose: This command calculates the ringing on the high portion of a signal.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the size of the record, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[H] an optional parameter. If [H] is specified, each ringing high value calculated is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[n] the record number.

The ringing is calculated as the dip below the 100% point following the peak of the signal. The maximum, minimum, and average values are returned. The addresses returned are the locations of the signal dips.

Examples:

AB/0	calculates the ringing (high) of RAMsize samples beginning at address 0 the trigger address).
AB	calculates the ringing (high) of RAMsize samples beginning at the address of the oldest data in memory.
AB100	calculates the ringing (high) of 100 samples beginning at the address of the oldest data in memory.
AB100/3200	calculates the ringing (high) of 100 samples beginning at address 3200.
ABR3	calculates the ringing (high) of record 3.
ABR7/100	calculates the ringing (high) of the first 100 samples of record 7.
ABR3/1000/50	calculates the ringing highs of 1000 samples beginning 50 locations from the start of record 3.
ABH	returns the calculated ringing values.
ABHR3	returns the calculated ringing values of record 3.

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Response Syntax:

BX = ringing maximum; BM = ringing minimum; BA = ringing average

BX = _-4.0000000E-002_(0010380)_BM = _-1.1000000E-002_(0001100)_
BA = _-3.20000000E-002<CR><LF>

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Command: AC (Calculate FFT)

Syntax:
AC[x][y][z][w]
ACR[n]/[x][y][z][w]

Purpose: The AC command performs a fast Fourier transform (FFT) on the sampled data. (See Appendix E for an overview of Fourier transform theory.)

Description: This command, the Hanning command (AH), and the Blackman-Harris command (AQ) analyze the sampled waveform in the frequency domain. An N-point FFT is performed, which "slices" the frequency spectrum of the waveform into N/2 frequency components, for a spectrum up to one-half the sampling frequency. Input requests immediately following these commands return the amplitude of each of the frequency components.

[x] V returns the amplitudes as relative voltage gain.
P returns the amplitudes as power in dB (decibels - milliwatts).
Not specified: defaults to V.

[y] X returns the maximum amplitude and its frequency (exclusive of the dc component).
S returns the signal-to-noise ratio (SNR), the total harmonic distortion (THD), the spurious free dynamic range (SFDR), and the signal-to-noise and distortion (SINAD) ratios in dBc [decibels referenced to the carrier input signal (fundamental)].
D returns the frequencies and amplitudes of the fundamental plus the first five harmonics.
Not specified: returns the amplitudes of each of the frequency components.

[z] 0 to RAMsize
Optional starting point. If no starting point is specified, the FFT is calculated from the address of the oldest data in memory, or the starting address of the record, respectively. When specified, the FFT is performed starting at this offset address.

[w] Nx where x = 7 to 12
This field specifies the size of the FFT to be performed as a power of 2. For example, if the [w] field is "N10," then a 1024 point transform is done (2^{10}).
Not specified: defaults to 10.

[n] the record number.

For [x] = V, the amplitudes are returned in decibels (dB) relative to the programmed input voltage range (V_R):

$$\text{Amplitude (dB)} = 20 \log V/V_R$$

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For [x] = P, the amplitudes are returned as power in decibels milliwatts (dBm) into 50 ohms.

Amplitude (dBm) = (10 log V^2/R) + 30
R = 50 ohms

To determine the power in decibel watts, subtract 30 from the returned values. To determine the power into a load other than 50 ohms, add 17 to the returned values, and subtract 10log(RL) where RL equals the resistance of the load.

For example, the power, in Watts, into 100 Ohms equals

(returned value) - 30 + 17 - 10log(100)

The frequency resolution of each slice is determined by dividing the sampling frequency by the size of the transform. The frequency spectrum is one-half the sampling frequency. For example, a waveform sampled at 10 MHz gives a frequency spectrum to 5 MHz.

Using a 1024 point transform, the resolution of each slice is:

10E6/1024 = 9.765625 kHz/slice

The first value returned corresponds to frequency 0 (or dc), the second value corresponds to 9.765625 kHz, the third value corresponds to 19.53125 kHz, and so on for each of the 512 slices.

Examples:

ACP100 — calculates the FFT starting at address 100, and returns the amplitudes as dBm. Since no size is specified, it defaults to 1024 (2^{10}), and a total of 512 (1024/2) values are returned.

ACXN10 — would return the maximum voltage in dB and its corresponding frequency. For a ±2-volt range and a measured voltage of 1.932V, the amplitude returned would be 20log(1.932/2.0) = -0.300457.

Response Syntax:

ACP100 — -1.6381000E+001;-5.0672000E+001;...;-2.7945000E+001;-3.0230000E+01;<CR><LF>

Assuming a sampling frequency of 10 MHz and a 1024 point transform (9.765625 KHz/slice), the first value returned, −16.381 dBm, corresponds to frequency 0 (or dc), the second value, -50.672 dBm, corresponds to 9.765625 KHz, etc. The data values are delimited by the terminator ";" (see the L command).

ACXN10 — FV=_-2.9878000E-001_+2.5000000E+006<CR><LF>

indicating a relative voltage gain of -0.29878 dB at 2.5 MHz.

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ACPX

FP=_+1.3117000E+001_+6.2500000E+005<CR><LF>

indicating a signal whose maximum amplitude is +13.117 dBm at 625 KHz.

ACR3/V

returns the voltage FFT of record 3.

ACS

THD=_-57.70_SNR=_54.13_SND=_50.48_SFR=_60.02 <CR><LF>

where THD is the total harmonic distortion, SNR is the signal-to-noise ratio, SND is the signal to noise and distortion ratio, and SFR is the spurious free dynamic range.

ACD

F1=_2.5390625E+005_A1=_-4.8594112E+000_
F2=_5.0781250E+005_A2=_-6.3733299E+001_
F3=_7.6171875E+005_A3=_-6.9593857E+001_
F4=_1.0156250E+006_A4=_-8.0922806E+001_
F5=_1.2695312E+006_A5=_-8.2780136E+001_
F6=_1.523438E+006_A6=_-8.34576243E+001
<CR><LF>

where F1 and A1 are the frequency and amplitude of the fundamental, F2/A2 are the frequency and amplitude of two times the fundamental, etc.

FFT Approximate Execution Times

[w] Field	Transform Size	AC command Exec. Time	AH command Exec. Time	AQ command Exec. Time
N7	128	64 ms	70 ms	80ms
N8	256	130 ms	138 ms	158 ms
N9	512	258 ms	276 ms	312 ms
N10	1024	516 ms	552 ms	624 ms
N11	2048	1.04 s	1.11 s	1.25 s
N12	4096	2.08 s	2.22 s	2.51 s

Transform Size	ACX command Exec. Time	ACS command Exec. Time	ACD command Exec. Time
128	18 ms	18 ms	30 ms
256	32 ms	34 ms	46 ms
512	60 ms	66 ms	76 ms
1024	120 ms	128 ms	138 ms
2048	240 ms	256 ms	264 ms
4096	490 ms	520 ms	532 ms

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[y] Options

The following [y] options to the FFT commands (AC, AH, and AQ) are special purpose routines for processing composite waveforms with multiple frequency components, and apply only to software V1.8 and later. They are not recommended for general use.

All of these options assume that [x] = V.

[y] = F

[y] = Z performs a quadratic log curve fit on the spectral data. This option returns the coefficients of the quadratic equation, the resonant frequency in radians (Wr) and Hertz (Fr), and the damping factor zeta (Ze). For [y] = Z, only Wr, Fr, and Ze are returned. The response syntax is:

Y = _[a]_[b](x)_[c](x²)_Wr = _[d]_Fr = _[e]_Ze = _[f]<cr><lf>

where

*[a], [b], [c] are the DC, X, and x^2 terms of the quadratic equation, respectively.
*[d], [e], [f] are the resonant frequency in radians, Hertz, and the damping factor, respectively.

* All values are in the exponential format: ±x.xxxE±xxx

Examples: The command ACZN12 would return the response

Wr = +6.863E+003 Fr = +1.092E+003 Ze = +1.155E-001

The command acfn11 would return the response

Y = -4.812E+001 -1.619E-003(X) -1.022E-006(X^2)
Wr = +6.863E+003 Fr = +1.092E+003 Ze = +1.155E-001

[y] = L determines the -3 to -18 dB frequencies, in -3 dB steps. The option returns the reference (low frequency) amplitude, and the -3 dB step frequencies. A frequency value of zero indicates the data did not drop below the respective dBs, relative to the reference. The response syntax is:

REF = _[a]_-03 = _[b]_-06 = _[b]_-09 = _[b]_-12 = _[b]_-15 = _[b]_-18 = _[b]<cr><lf>

where

[a] = reference amplitude in dBs
[b] = -3 dB to -18 dB frequencies

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Example: The command ACLN12 would return the response

REF= -4.86714E+001 -03= 1.15463E+003 -06= 1.77116E+003 -09= 0.00000E+000
-12= 0.00000E+000 -15= 0.00000E+000 -18=0.00000E+000

[y] = K determines the peaks of the composite waveform, and returns the number of peaks found, followed by the amplitude, frequency index, and phase angle of each of the peaks. The actual frequency of a value is [(sampling frequency/FFT size) × frequency index]. For example, if the sampling frequency were 10 KHz, and a 1024-point FFT was performed, a frequency index of 13 indicates a frequency of:

(10 KHz / 1024) × 13 = 126.95 Hz

The response syntax is:

[a][b]/[c]/[d];[b]/[c]/[d];...[b]/[c]/[d]<cr><lf>

where

[a] = a four-digit integer indicating the number of peaks to follow.

[b] = the magnitude in dB of the peak, in the format: ±xxx.xx.

[c] = a four-digit integer indicating the frequency index.

[d] = [phase angle in degrees (±180°), in the format: ±xxx.xx.

Example: The command ACKN11 would return the response

0398-049.02/0007/-058.04;-048.32/0010/-149.75;-048.60/0013/+117.09;
...; -049.33/0237/-014.43;-048.92/0240/-111.46;-049.16/0242/-046.57

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Command: AD (Difference)

Syntax:
AD[x]/[y][Sz]
ADR[n]/[x]/[y][Sz]

Purpose: This command returns the difference between successive data points.

Description:

[x] the number of samples, from 1 to 1000 maximum. If [x] is not specified, it defaults to 1.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

Examples:

AD10/0	returns 10 values, beginning with value 1 - value 0, and ending with value 11 - value 10.
AD2/20	returns 2 values representing value 21 - value 20, and value 22 - value 21.
ADR2/100	returns the difference values for the first 100 samples of record 2.
ADR3/10/200	returns 10 difference values beginning 200 locations from the start of record 3.
AD100/0S4	returns the difference of every fourth memory location, for 100 values, beginning at address 0.

Response Syntax:

If the delimiter was defined as a semi-colon (by the L command), the command AD3 could return:

-1.6000000E-002;+2.4000000E-002;+0.0000000E+000;<CR><LF>

If the delimiter was defined as a space (by the L command), the command ADR5/3 could return:

-1.6000000E-002_+2.4000000E-002_+0.0000000E+000_<CR><LF>

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Command: AE Ringing (low)

Syntax: AE[H][x]/[y]
AE[H]R[n]/[x]/[y]

Purpose: This command calculates the ringing on the low portion of a signal.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[H] an optional parameter. If [H] is specified, each ringing low value calculated is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[n] the record number.

Ringing is calculated as the rise above the 0% point immediately following the valley of the signal. The maximum, minimum, and average values are returned. The addresses returned are the rise locations.

Examples:

AE/0	calculates the ringing (low) of RAMsize samples beginning at address 0 (the trigger address).
AE	calculates the ringing (low) of RAMsize samples beginning at the address of the oldest data in memory.
AE100	calculates the ringing (low) of 100 samples beginning at the address of the oldest data in memory.
AE100/3200	calculates the ringing (low) of 100 samples beginning at address 3200.
AER3	calculates the ringing (low) of record 3.
AER7/100	calculates the ringing (low) of the first 100 samples of record 7.
AER3/1000/50	calculates the ringing low of 1000 samples beginning 50 locations from the start of record 3.
AEH	returns the calculated ringing values.
AEHR2	returns the calculated ringing values of record 2.

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Response Syntax:

EX = ringing maximum; EM = ringing minimum; EA = ringing average
EX=_+2.2000000E-002_(0012345)_EM=_+2.3000000E-003_(0005432)_EA=_+1.2000000E-002<CR><LF>

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Command: AF (Fall time)

Syntax:
AF[H][x]/[y]
AF[H]R[n]/[x]/[y]

Purpose: This command calculates the fall times of the sampled signal.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[H] an optional parameter. If [H] is specified, each rise time calculated is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[n] the record number.

The fall time is the time it takes for the signal to complete the transition from 90% to 10% of its steady state value. The maximum, minimum, and average fall times are returned. The addresses returned are one location prior to where the signal crossed the 90% point.

Examples:

AF/0	calculates the fall times of RAMsize samples beginning at address 0 (the trigger address).
AF	calculates the fall times of RAMsize samples beginning at the address of the oldest data in memory.
AF100	calculates the fall times of 100 samples beginning at the address of the oldest data in memory.
AF100/3200	calculates the fall times of 100 samples beginning at address 3200.
AFR3	calculates the fall times of record 3.
AFR7/100	calculates the fall times of the first 100 samples of record 7.
AFR3/1000/900	calculates the fall times of 1000 samples beginning 900 locations from the start of record 3.
AFH	returns the calculated fall times.
AFHR2	returns the calculated fall times of record 2.

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Response Syntax:

FX = maximum fall time, FM = minimum fall time,
FA = average fall time

FX=_+1.1583000E-006_(0001366)_FM=_+9.9405000E-007_(0000306
)_
FA=_+1.1057000E-006<CR><LF>

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Command: AG (Record Operations)

Syntax: AG[x][/y]. . .
AG[x]M[/w][/y][/z]

Purpose: This command creates a new record by performing various operations on the records stored in memory.

Description: [x] is a single letter, which must be one of the following:

A creates a new record which is the average of the records specified by the [/y] option. If [/y] is not specified, the new record created will be the average of all the records stored.

D creates a new record which is the difference between the two records specified by the [/y] option. If [/y] is not specified, the new record created will be the difference between record 1 and record 2 [record 1 - record 2 (AGD/1/2)]. If more than two records are specified, an error will be generated.

E creates a new record which is the difference between the maximum and minimum values of the records specified by the [/y] option. If [/y] is not specified, the new record created will be the difference values of all the records stored.

M creates a new record which is the minimum values of the records specified by the [/y] option. If [/y] is not specified, the new record created will be the minimum values of all the records stored.

X creates a new record which is the maximum values of the records specified by the [/y] option. If [/y] is not specified, the new record created will be the maximum values of all the records stored.

[/y] defines which records are to be operated on. For example, AGA/1/7/5 will create a new record which is the average of records 1, 7, and 5. [/y] can also be specified as /R_1TR_2, which defines records R_1 through R_2. for example AGA/2/5T7/9 will average records 2, 5 through 7, and record 9. R_2 must be greater than R_1 or an error will be generated.

The M option for this command AG[x]M[/w][/y][z] allows the operations to be performed on records at regularly spaced intervals. [x] is the same as defined above. [/w] is the record interval, [/y] is the beginning record, and [z] is the number of records to be operated on. For example, AGAM/3/2/5 will average every third record, beginning with record 2, for a total of five records. The newly created record will then be the average of records 2, 5, 8, 11, and 14.

The new record created will be appended to the end of the last record in memory. For example, if 16 records of 10000 samples each (0 through 159999, or 160000 samples) were taken, the new record would begin at address 160000

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and extend 10000 samples to address 169999. All the other Analyze commands could then operate on it as record 17. For example, if an AGA command were issued, the newly created record would be the average value of the 16 records. If an AKR17 command was then issued, the peak to peak values of the newly created record 17 (the average of the 16 sampled records) would be calculated.

If there is not enough memory left over to create a new record, the last record in memory will be overwritten with the new record. For example, if the card had 256K of memory (262144) and 26 records of 10000 samples each (260000 total) were taken, issuing an AGA command would overwrite record 26 with the newly calculated values.

When creating the new record, the new values are the applicable operation performed on the same relative values of the records specified. For example, if AGA/1/2/3 were specified, then the first value of the new record would be the sum of the first values of records 1 through 3 divided by 3. The second value of the new record would be the sum of the second values of records 1 through 3 divided by 3, etc.

Except for the overwrite condition described above, the newly created record will always be one greater than the number of records specified by the Collect command. For example, if ten records are taken, the new record is record 11.

Examples:

AGA/1/5 creates the new record as the average of records 1 and 5.

AGE/1T9 creates the new record as the difference between the maximum value found in each respective locations of records 1 through 9, and the minimum value found in each respective location.

AGM creates the new record as the minimum value found in each respective location of all the records.

AGD/5/4 creates the new record as the difference between each respective location of record 5 minus record 4.

AGX/2/5T7/9
creates the new record as the maximum value found in each respective location of records 2, 5 through 7, and 9.

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Command: AH (Calculate FFT/Hanning)

Syntax:
AH[x][y][z][w]
AHR[n][x][y][z][w]

Purpose: The AH (Calculate FFT/Hanning) command is identical to the AC command, and calculates a fast Fourier transform (FFT) with Hanning leakage-reduction compensation.

Description: The Hanning function reduces the leakage inherent in the fast Fourier transform (see Appendix E).

Each of the time domain points are first multiplied by the following term before it is transformed into the frequency domain:

$$\frac{1}{2} - \frac{1}{2} \cos [\, 2\pi t / N \,]$$

where t = 0 to N, and N = the number of points in the transform (e.g. 1024).

Response Syntax: Refer to the AC command response. Responses to the AH and the AC commands have the same format.

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Command: AI (Integrate)

Syntax: AI[x]/[y][Sz]
AIR[n]/[x]/[y][Sz]

Purpose: This command returns the sum of successive data points.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

Examples:

AI/0	returns the sum of RAMsize samples beginning at address 0 (the trigger address).
AI	returns the sum of RAMsize samples beginning at the address of the oldest data in memory.
AI20	returns the sum of 20 samples beginning at the address of the oldest data in memory.
AI20/100	returns the sum of 20 samples beginning at address 100.
AIR20	returns the sum of record 20.
AIR20/100	returns the sum of the first 100 values of record 20.
AIR2/5/10	returns the sum of 5 values beginning 10 locations from the start of record 2.
AI/0S4	returns the sum of RAMsize/4 samples, for every fourth location, beginning at address 0.

NOTE: Multiplying the sum by the number of samples gives the area under the curve normalized to a delta time interval of 1 (rectangular approximation).

Response Syntax: IT=_+4.0000000E-001<CR><LF>

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Command: AK (Peak-to-Peak)

Syntax:
AK[H][x]/[y][w]
AK[H]R[n]/[x]/[y][w]

Purpose: This command calculates the peak-to-peak voltage or the 100%, 90%, 10% or 0% values of the sampled signal.

Description:

[H] an optional parameter. If [H] is specified, each value calculated is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[n] the record number.

[w] an optional parameter which specifies the data to be returned. If [w] is not specified, the peak-to-peak voltages will be returned. If the [w] option is followed by a 'Z', the zero reference point of the calculations is based on absolute zero, instead of the floating reference (max + min) / 2.

w	values returned
0	100% (addresses are of the peak value of the pulse)
N	90% (addresses are of the peak value of the pulse)
T	10% (addresses are of the minimum value of the pulse)
Z	0% (addresses are of the minimum value of the pulse)

The peak-to-peak voltage is determined as the difference between the steady-state high of the signal (100% point), and the steady-state low (0% point). The maximum, minimum, and average peak-to-peak voltages are returned. The addresses returned are the addresses of the peak value of the pulse.

Examples:

AK/0	calculates the peak-to-peaks of RAMsize samples beginning at address 0 (the trigger address).
AK	calculates the peak-to-peaks of RAMsize samples beginning at the address of the oldest data in memory.
AK100	calculates the peak-to-peaks of 100 samples beginning at the address of the oldest data in memory.
AK100/3200	calculates the peak-to-peaks of 100 samples beginning at address 3200.

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AKR3	calculates the peak-to-peaks of record 3.
AKR7/100	calculates the peak-to-peaks of the first 100 samples of record 7.
AKR3/1000/900	calculates the peak-to-peaks of 1000 samples beginning 900 locations from the start of record 3.
AKH	returns the calculated peak-to-peak values.
AKHR3	returns the calculated peak-to-peak values of record 3.
AK12340	calculate the 100% values of 1234 samples beginning at the address of the oldest data in memory.
AK1E3/0N	calculate the 90% values of 1000 samples beginning at address 0 (the trigger address).
AKR7/100/0T	calculate the 10% values of 100 samples beginning at address 0 of record 7.
AKHR3Z	return the calculated 0% values of record 3.

Response Syntax:

aX = maximum, aM = minimum, aA = average. 'a' is K, O, N, T, or Z, indicating the type of values returned.

Peak-to-peak values:

KX=_+1.4080000E+001_(0001196)_KM=_+1.3280000E+001_(0000336)_KA=_+1.3847000E+001<CR><LF>

One hundred percent values:

OX=_+8.9468384E-001_(0000148)_OM=_+8.8909912E-001_(0008247)_ OA=_+8.9339748E-001<CR><LF>

Ninety percent values:

NX=_+7.1676636E-001_(0003747)_NM=_+7.1142578E-001_(0004147) _NA=_+7.1530121E-001<CR><LF>

Ten percent values:

TX=_-7.0578003E-001(0001447)_TM=_-7.1118164E-001_(0007147) _TA=_-7.0960120E-001<CR><LF>

Zero percent values:

ZX=_-8.8354492E-001(0001447)_ZM=_-8.8931274E-001_(0009147)_ ZA=_-8.8769747E-001<CR><LF>

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Command: AL (single frequency discrete Fourier transform (DFT))

Syntax:
AL[x]/[y]F[z][w]
ALR[n]/[x]/[y]F[z][w]

Purpose: This command performs a discrete Fourier transform (DFT) for a single specified frequency. That is, it performs a spectral analysis to determine the amplitude and phase of a single frequency within an input signal.

Description:

[x] the number of samples to calculate the DFT across, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to +RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively. (Address 0 is the trigger address.)

[n] the record number.

[z] the desired frequency to calculate the DFT with. If Fz is omitted, an error is generated.

[w] an optional parameter, which must be either S or D:
S calculates the DFT using single precision floating point values (default).
D calculates the DFT using double precision floating point values.

To prevent numeric overflow in the calculations, double precision calculations should be used if
(number of samples [x]) * (specified frequency [z]) > $1.0e^{10}$

If overflow occurs, the value(s) returned in the response will be an ASCII 'NaN', indicating the result is 'Not a Number'.

Response Syntax: MG=_+6.988301E-001_PH=_+2.7993540E+000<CR><LF>

where MG is the amplitude in volts RMS, and PH is the phase in radians.

Examples:

AL100/200F100E3	calculate the 100 KHz DFT of 100 samples beginning at address 200, with single precision.
AL1000/0F2500D	calculate the 2500 Hz DFT of 1000 samples beginning at address 0 (the trigger address), with double precision.
ALR5/10E3/0F1.1E3S	calculate the 1.1 KHz DFT of 10000 samples beginning at address 0 of record 5, with single precision.

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Approximate Execution Times (in seconds)

# of Samples	Single Precision	Double Precision
100	0.011	0.013
1000	0.077	0.108
10000	0.730	1.060
100000	6.40	6.40

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Command: AM (Minimum voltage)

Syntax:
AM[x]/[y][Sz]
AMR[n]/[x]/[y][Sz]

Purpose: This command returns the minimum voltage stored in memory.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to +RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

Examples:

AM/0	returns the minimum voltage of RAMsize samples beginning at address 0.
AM	returns the minimum voltage of RAMsize samples beginning at the address of the oldest data in memory.
AM8000	returns the minimum voltage of 8000 samples beginning at the address of the oldest data in memory.
AM20/-10	returns the minimum voltage of 20 samples beginning 10 samples prior to address 0 (the trigger address) and ending 9 samples after the trigger.
AMR20	returns the minimum value in record 20.
AMR20/100	returns the minimum value of the first 100 samples in record 20.
AMR3/10/200	returns the minimum value of 10 samples beginning 200 locations from the start of record 3.
AM/0S4	returns the minimum value of RAMsize/4 samples, for every fourth memory location, beginning at address 0.

Response Syntax: Minimum value of data in memory

MV=_-8.8800000E+000_(0000410)<CR><LF>

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Command: AN (Maximum negative transition)

Syntax:
AN[x]/[y][Sz]
ANR[n]/[x]/[y][Sz]

Purpose: This command returns the maximum negative voltage change between any two successive samples in memory.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

Examples:

AN/0	returns the maximum negative transition found in RAMsize samples beginning at address 0 (the trigger address).
AN	returns the maximum negative transition found in RAMsize samples beginning at the address of the oldest data in memory.
AN100	returns the maximum negative transition found in 100 samples beginning at the address of the oldest data in memory.
AN100/300	returns the maximum negative transition found in 100 samples beginning at address 300.
ANR1	returns the maximum negative transition in record 1.
ANR11/1000	returns the maximum negative transition found in the first 1000 samples of record 11.
ANR3/10/200	returns the maximum negative transition found in 10 samples beginning 200 locations from the start of record 3.
AN/0S4	returns the maximum negative transition found between every fourth memory location, beginning at address 0, for RAMsize/4 samples.

Response Syntax: Maximum negative transition

NT=_-4.8000000E+000_(0001042)<CR><LF>

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Command: AO (Overshoot)

Syntax:
AO[H][x]/[y]
AO[H]R[n]/[x]/[y]

Purpose: This command calculates the overshoots of the sampled signal.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[H] an optional parameter. If [H] is specified, each overshoot calculated is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[n] the record number.

The overshoot is defined as the difference between the maximum value of a signal and its 100% point. The maximum, minimum, and average overshoots are returned. The addresses returned are the locations of the overshoots.

Examples:

AO/0	calculates the overshoots of RAMsize samples beginning at address 0 (the trigger address).
AO	calculates the overshoots of RAMsize samples beginning at the address of the oldest data in memory.
AO100	calculates the overshoots of 100 samples beginning at the address of the oldest data in memory.
AO100/3200	calculates the overshoots of 100 samples beginning at address 3200.
AOR3	calculates the overshoots of record 3.
AOR7/100	calculates the overshoots of the first 100 samples of record 7.
AOR3/1000/900	calculates the overshoots of 1000 samples beginning 900 locations from the start of record 3.
AOH	returns the calculated overshoot values.
AOHR2	returns the calculated overshoot values of record 2.

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Response Syntax:

OX = maximum overshoot; OM = minimum overshoot; OA = average overshoot

OX=_+1.2800000E+000_(0000336)_OM=_+4.2000000E-002_(0001275)_
OA=_+7.1000000E-002<CR><LF>

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Command: AP (Maximum positive transition)

Syntax:
AP[x]/[y][Sz]
APR[n]/[x]/[y][Sz]

Purpose: This command returns the maximum positive voltage change between any two successive points in memory.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

Examples:

AP/0	returns the maximum positive transition found in RAMsize samples beginning at address 0 (the trigger address).
AP	returns the maximum positive transition found in RAMsize samples beginning at the address of the oldest data in memory.
AP100	returns the maximum positive transition found in 100 samples beginning at the address of the oldest data in memory.
AP100/300	returns the maximum positive transition found in 100 samples beginning at address 300.
APR23	Returns the maximum positive transition found in record 23.
APR23/100	returns the maximum positive transition found in the first 100 samples of record 23.
APR1/10/100	returns the maximum positive transition found in 10 samples beginning 100 locations from the start of record 1.
AP/0S4	returns the maximum positive transition found between every fourth memory location, beginning at address 0, for RAMsize/4 samples.

Response Syntax: Maximum positive transition

PT=_+3.2800000E+000_(0002082)<CR><LF>

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Command: AQ (Calculate FFT/Blackman-Harris)

Syntax:
AQ[x][y][z][w]
AQR[n][x][y][z][w]

Purpose: The AQ (Calculate FFT/Blackman-Harris) command is identical to the AC command, and calculates a fast Fourier transform (FFT) with Blackman-Harris leakage-reduction compensation.

Description: The Blackman-Harris function reduces the leakage inherent in the fast Fourier transform (see Appendix E). It also resolves closer peaks in the frequency spectrum than the Hanning window.

Each of the time domain points is first multiplied by the following term before it is transformed into the frequency domain:

$$0.35875 - 0.48829 \cos\left(\frac{2\pi t}{N}\right) + 0.14128 \cos\left(\frac{2\pi * 2t}{N}\right) - 0.01168 \cos\left(\frac{2\pi * 3t}{N}\right)$$

where t = 0 to N, and N = the number of points in the transform (e.g. 1024).

Response Syntax: Refer to the AC command response. Responses to the AQ and the AC commands have the same format.

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Command: AR (Rise Time)

Syntax:
AR[H][x]/[y]
AR[H]R[n]/[x]/[y]

Purpose: This command calculates the rise times of the sampled signal.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[H] an optional parameter. If [H] is specified, each rise time calculated is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[n] the record number.

The rise time is determined as the time it takes for the signal to complete the transition from 10% to 90% of its steady-state value. The maximum, minimum, and average rise times are returned. The addresses returned are one location prior to where the signal crosses the 10% point.

Examples:

AR/0	calculates the rise times of RAMsize samples beginning at address 0 (the trigger address).
AR	calculates the rise times of RAMsize samples beginning at the address of the oldest data in memory.
AR100	calculates the rise times of 100 samples beginning at the address of the oldest data in memory.
AR100/3200	calculates the rise times of 100 samples beginning at address 3200.
ARR3	calculates the rise times of record 3.
ARR7/100	calculates the rise times of the first 100 samples of record 7.
ARR3/1000/50	calculates the rise times of 1000 samples beginning 50 locations from the start of record 3.
ARH	returns the calculated rise times.
ARHR2	returns the calculated rise times of record 2.

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Response Syntax:

RX = maximum rise time, RM = minimum rise time,
RA = average rise time

RX=_+1.4375000E-011_(0000466)_RM=_+1.2875000E-011_(000032
6)_RA=_+1.3808000E-011<CR><LF>

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Command: AS (Statistics)

Syntax:
AS[x]/[y][z]
ASR[n]/[x]/[y][z]

Purpose: This command returns the mean, standard deviation and percentage of data within ±N*sigma of the mean.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[z] Px, an optional parameter, where x is 1 to 9, and specifies the PS return value to be the percentage of data within ±x*σ of the mean. If [z] is not specified, it defaults to ±1.

[n] the record number.

The mean of the signal is defined as

$$MN = \frac{\left(\sum_{i=1}^{N} x_i\right)}{N}$$

where N is the number of samples, and x_i is the ith data point. Note that the mean is equivalent to the average value of the signal. The standard deviation (σ, sigma) is defined as

$$\sigma = \sqrt{\frac{1}{n}\sum_{i=1}^{N}(x_i - MN)^2}$$

For a Gaussian (bell curve) distribution, the probability of finding the value between ±σ is 68.13%. For ±2σ, the probability is 95.5%, and for ±3σ, the probability is 99.7%. For the example below, 98.1% of the data falls within ±0.9801841 volts of the mean, 0.049187963.

Response Syntax: MN = mean (in volts); DS = standard deviation (in volts); PS = percentage of data within ±N*σ.

MN=_+4.9187963E-002_DS=_+9.8018410E-001_PS=_+98.1<CR><LF>

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Examples:

AS	returns the mean, standard deviation and ±1σ percentage of RAMsize samples.
AS1000	returns the mean, standard deviation and ±1σ percentage of the first 1000 samples.
AS1000/500P2	returns the mean, standard deviation and ±2σ percentage of 1000 samples beginning 500 locations from the trigger (address 0).
ASR2	returns the mean, standard deviation and ±1σ percentage of record 2.
ASP3	returns the mean, standard deviation and ±3σ percentage of RAMsize samples.
AS/0S4	returns the mean, standard deviation and ±1σ percentage of RAMsize/4 samples, for every fourth sample, beginning at address 0.

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Command: AT (True RMS voltage)

Syntax:
AT[x]/[y][Sz]
ATR[n]/[x]/[y][Sz]

Purpose: This command calculates the RMS value of the data in memory.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

The true RMS (TRMS) is defined as the square root of the sum of the square of each data point divided by the number of samples.

Examples:

AT/0	calculates the TRMS value of RAMsize samples beginning at address 0 (the trigger address).
AT	calculates the TRMS value of RAMsize samples beginning at the address of the oldest data in memory.
AT100	calculates the TRMS value of 100 samples beginning at the address of the oldest data in memory.
AT100/300	calculates the TRMS value of 100 samples beginning at address 300.
ATR1	returns the TRMS value of record 1.
ATR99/88	returns the TRMS value of the first 88 samples of record 99.
ATR3/100/200	returns the TRMS value of 100 samples beginning 200 locations from the start of record 3.
AT/0S4	calculates the TRMS value of RAMsize/4 samples, for every fourth memory location, beginning at address 0.

Example True RMS calculation:

The TRMS of three voltages: 0.25V dc, 0.5V dc, and 0.25V dc is

$\surd \{[(.25 \times .25) + (.5 \times .5) + (.25 \times .25)] / 3\} = .35355V$ dc

Response Syntax: True RMS value

TR=_+4.5134000E+000<CR><LF>

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Command: AU (Undershoot)

Syntax:
AU[H][x]/[y]
AU[H]R[n]/[x]/[y]

Purpose: This command calculates the undershoots of the sampled signal.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[H] an optional parameter. If [H] is specified, each undershoot calculated is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[n] the record number.

The undershoot is defined as the difference between the 0% value of a signal and its minimum point. The maximum, minimum, and average undershoots are returned. The addresses returned are the locations of the undershoots.

Examples:

AU/0	calculates the undershoots of RAMsize samples beginning at address 0 (the trigger address).
AU	calculates the undershoots of RAMsize samples beginning at the address of the oldest data in memory.
AU100	calculates the undershoots of 100 samples beginning at the address of the oldest data in memory.
AU100/3200	calculates the undershoots of 100 samples beginning at address 3200.
AUR3	calculates the undershoots of record 3.
AUR7/100	calculates the undershoots of the first 100 samples of record 7.
AUR3/1000/50	calculates the undershoots of 1000 samples beginning 50 locations from the start of record 3.
AUH	returns the calculated undershoots.
AUHR2	returns the calculated undershoots of record 2.

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Response Syntax:

UX = maximum undershoot; UM = minimum undershoot; UA = average undershoot)

UX = _-9.6000000E-002_(0000855)_UM = _-3.60000000E-002_ (0000123)_UA = _-5.4000000E-002<CR><LF>

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Command: AV

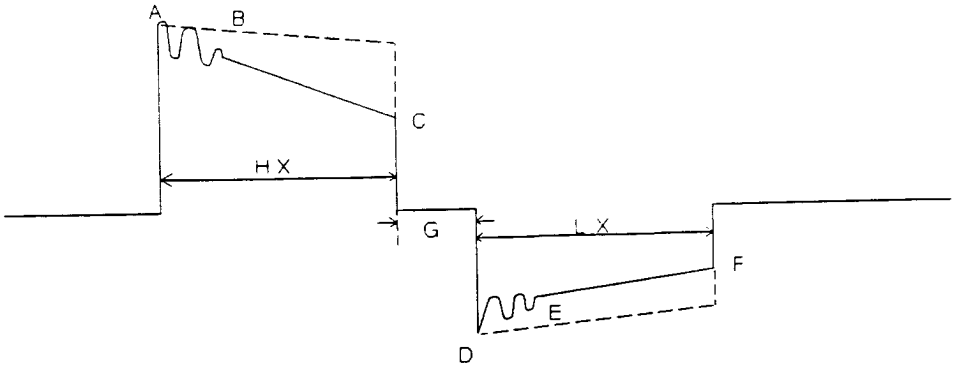
Syntax: AV[x]/[y]

Purpose: This command calculates specific parameters for a pulse of the type shown below.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from - RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.



Response Syntax: [A]_Ph=_[B]_Pl=_[B]_A=_[C]_[D]_B=_[C]_D=_[C]_[D]_E=_[C]_F=_[C]_[D]_G=_[C]_HX=_[C]_[D]_HM=_[C]_[D]_LX=_[C]_[D]_LM=_[C]_[D] <CR><LF>

[A] Error if Ph <>1 or Pl <>1
Pulse if Ph=Pl=1

[B] XXXXXXX - Integer value indicating the number of pulses (high/low) seen.

[C] ±X.XXXXXXXE±XXX - Floating point number.

[D] XXXXXXX - Integer value corresponding to the address of the measured value.

Example Response:

PULSE Ph= 0000001 Pl= 0000001 A= +7.3876953E+000 (0000000) B= +7.3864746E+000 C= +1.9580078E+000 (0039999) D= -3.4960937E+000 (0044001) E= -3.4988403E+000 F= -5.1757812E-001 (0083997) G= +4.0000000E-004 HX= +4.0000300E-003 (0262142) HM=

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+4.0000300E-003 (0262142) LX = +3.9999448E-003 (0043998) LM =
+3.9999448E-003 (0043998)

Ph The number of positive pulses detected. (See Note 1.)

Pl The number of negative pulses detected. (See Note 1.)

A The maximum positive signal amplitude (and address).

B The average of 10 values beginning 10 µs after "A."

C Positive knee value (and address). (See Note 2.)

D The maximum negative signal amplitude (and address)

E The average of 10 values beginning 10 µs after "D."

F Negative knee value (and address). (See Note 2.)

G The time the signal is nominally zero between "C" and "D."

HX The pulse width high maximum time (and address).

HM The pulse width high minimum time (and address). (See Note 3.)

LX The pulse width low maximum time (and address).

LM The pulse width low minimum time (and address). (See Note 3.)

NOTES:

1 If more than one high or one low pulse is detected, the response will lead off with "error." Multiple pulse detection is provided to detect signal oscillation. Any positive edge greater than "B"/2, followed later by a negative edge "B"/2 is considered a high pulse. Similarly for Pl using "E"/2. When scanning for pulses, the program uses a ±16 count hysteresis around the mid-point values to prevent noise from erroneously causing an extra pulse to be detected.

2 "C" and "F" must be greater than 2.5% of the programmed input range for correct command operation.

3 If only one high (or low) pulse is detected, the minimum values will equal the maximum values. Otherwise, the program will attempt to calculate a minimum oscillation pulse width.

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Command: AW (Pulse width)

Syntax:
AW[H][x][y]/[z]
AW[H][x]R[n]/[y]/[z]

Purpose: This command calculates various parameters relating to the pulse widths of a waveform. This command is identical to the AZ command, except that the "zero" reference point is taken as

[(maximum value) + (minimum value)] / 2

Description:

[x] a single letter, which must be one of the following:

[x]	returns:
G	the maximum, minimum, and average times the pulse is high
L	the maximum, minimum, and average times the pulse is low
P	the maximum, minimum, and average periods
F	the maximum, minimum, and average frequencies
D	the maximum, minimum, and average duty cycles. The duty cycle is defined as

[(pulse high time)/(pulse high time + pulse low time)] * 100

[y] the number of samples, from 1 to RAMsize. If [y] is not specified, it defaults to RAMsize or the size of the record, respectively.

[H] an optional parameter. If [H] is specified, each calculated value is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[z] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[n] the record number.

Examples:

AWG1000	returns the calculated values of the first 100 samples beginning at the address of the oldest data in memory.
AWG1000/100	returns the calculated values of the first 100 samples beginning at address 100.
AWGR3	returns the calculated values of record 3.
AWGR3/1000	returns the calculated values of the first 1000 samples of record 3.

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AWGR3/1000/100
returns the calculated values of the first 1000 samples of record 3 beginning 100 locations from the start of record 3.

Response Syntax:

WX = maximum, WM = minimum, WA = average.

Cmd Response

AWG WX=_+5.1001334E-006_(0068166)_WM=_+4.8788647E-006_(0123447)_WA=_+4.9872106E-006

AWL Wx=_+5.1376237E-006_(0074826)_Wm=_+4.9135697E-006_(0088147)_Wa=_+5.0272752E-006

AWP Px=_+1.0107840E-005_(0000068)_Pm=_+9.9928246E-006_(0002772)_Pa=_+1.0014554E-006

AWF Qx=_+1.0007181E+005_(0002772_Qm=_+9.8933106E+004_(0000068)_Qa=_+9.9854673E+004

AWD Dx=_+5.0888675E+001_(0072072)_Dm=_+4.8714149E+001_(0074777)_Da=_+4.9800348E+001

AWHG250 +4.9213997E-006;+4.8977528E-006;<CR><LF>

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Command: AX (Maximum voltage)

Syntax:
AX[x]/[y][Sz]
AXR[n]/[x]/[y][Sz]

Purpose: This command returns the maximum voltage stored in memory.

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[Sz] Optional parameter specifying a step size; where [z] = 1 to 65536. If [z] is not specified, it defaults to 1.

[n] the record number.

Examples:

AX/0	returns the maximum voltage of RAMsize samples, beginning at address 0 (the trigger address).
AX	returns the maximum voltage of RAMsize samples, beginning at the address of the oldest data in memory.
AX8000	returns the maximum voltage of 8000 samples, beginning at the address of the oldest data in memory.
AX200/100	returns the maximum voltage of 200 samples, beginning at address 100.
AXR7	returns the maximum voltage in record 7.
AXR7/20	returns the maximum voltage of the first 20 samples in record 7.
AXR2/10/100	returns the maximum voltage of 10 samples beginning 100 locations from the start of record 2.
AX/0S4	returns the maximum value of RAMsize/4 samples, for every fourth memory location, beginning at address 0.

Response Syntax: Maximum value of data in memory

XV=_+9.5200000E+000_(0001850)<CR><LF>

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Command: AY

Syntax:
AY[x]/[y]
AYR[n]/[x]/[y]

Purpose: This command returns the number of complete cycles found in memory. One complete cycle is the interval between consecutive low-to-high transitions of the signal. The "zero" reference point is taken as

(maximum value + minimum value) / 2

Description:

[x] the number of samples, from 1 to RAMsize. If [x] is not specified, it defaults to RAMsize or the record size, respectively.

[y] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[n] the record number.

Response Syntax: CY = _XXXXXXX<CR><LF> where XXXXXXX is the number of cycles found.

Examples:

AY	returns the number of cycles found in memory.
AY1000	returns the number of cycles found in the first 1000 samples.
AYR3	returns the number of cycles found in record 3.
AYR3/1000/500	returns the number of cycles found in 1000 samples beginning 500 locations from the start of record 3.

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Command: AZ (Zero Crossing Times)

Syntax:
AZ[H][x][y]/[z]
AZ[H][x]R[n]/[y]/[z]

Purpose: This command calculates various parameters relating to the pulse widths of a waveform. This command is identical to the AW command, except that the "zero" reference point is taken as absolute zero.

Description: [x] a single letter, which must be one of the following:

[x]	returns:
G	the maximum, minimum, and average times the pulse is high
L	the maximum, minimum, and average times the pulse is low
P	the maximum, minimum, and average periods
F	the maximum, minimum, and average frequencies
D	the maximum, minimum, and average duty cycles. The duty cycle is defined as [(pulse high time)/(pulse high time + pulse low time)] * 100

[y] the number of samples, from 1 to RAMsize. If [y] is not specified, it defaults to RAMsize or the size of the record, respectively.

[H] an optional parameter. If [H] is specified, each calculated value is returned (up to 2000 maximum). Each data value will be delimited with the character specified by the L command. The response data is the same format as for the AD command.

[z] optional starting address from -RAMsize to + RAMsize. If [y] is not specified, it defaults to the address of the oldest data in memory, or the starting address of the record, respectively.

[n] the record number.

Examples:

AZG1000	returns the calculated values of the first 100 samples, beginning at the address of the oldest data in memory.
AZG1000/100	returns the calculated values of the first 100 samples beginning at address 100.
AZGR3	returns the calculated values of record 3.
AZGR3/1000	returns the calculated values of the first 1000 samples of record 3.

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AZGR3/1000/100 returns the calculated values of the first 1000 samples of record 3 beginning 100 locations from the start of record 3.

Response Syntax: ZX = maximum, ZM = minimum, ZA = average.

AZG ZX = _ + 5.1001334E-006_(0068166)_ZM = _ + 4.8788647E-006_ (0123447)_ZA = _ + 4.9872106E-006

AZL Zx = _ + 5.1376237E-006_(0074826)_Zm = _ + 4.9135697E-006_ (0088147)_Za = _ + 5.0272752E-006

AZP PX = _ + 1.0107840E-005_(0000068)_PM = _ + 9.9928246E-006_ (0002772)_PA = _ + 1.0014554E-006

AZF QX = _ + 1.0007181E + 005_(0002772_QM = _ + 9.8933106E + 004_ (0000068)_QA = _ + 9.9854673E + 004

AZD DX = _ + 5.0888675E + 001_(0072072)_DM = _ + 4.8714149E + 001_ (0074777)_DA = _ + 4.9800348E + 001

AZHG250 + 4.9213997E-006; + 4.8977528E-006; <CR> <LF>

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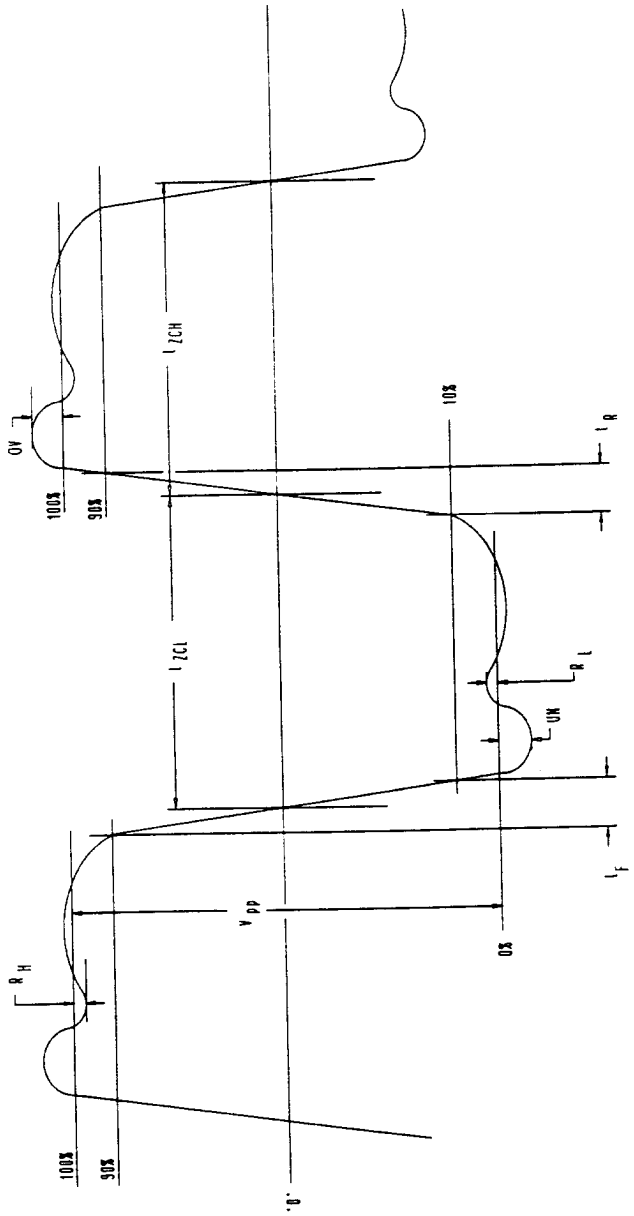

OV = OVERSHOOT
UN = UNDERSHOOT
V_{pp} = PEAK-TO-PEAK VOLTAGE
t_R = RISE TIME 10% TO 90%
t_f = FALL TIME 90% TO 10%
t_{ZCH} = ZERO CROSSING HIGH TIME
t_{ZCL} = ZERO CROSSING LOW TIME
R_H = RINGING ON THE HIGH BIT
R_L = RINGING ON THE LOW BIT

Figure 4: A (Analyze) Command Responses

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Command: B (Backplane interrupt)

Syntax: B[z]

Purpose: This command defines which condition will generate a Request True interrupt to the system controller.

Description: [z] a single letter, which must be one of the following:

[z]	Interrupt condition
A	Armed
C	Analyze command complete
D	Disable the interrupt (default)
M	Measurement complete
R	Record complete
T	Triggered

If [z] is not specified, an interrupt will be generated on measurement complete (M).

If programmed, the backplane interrupt command generates a Request True interrupt to the VXIbus system controller. For the VX4240, the interrupt condition is enabled when a Trigger command is received (except for the BC command). Once the interrupt has occurred, it will remain active until either the interrupt is acknowledged by the system controller, or the module is reset.

Condition	Interrupt occurs
armed	when the module is armed by the Trigger command. If the external arm signal has been programmed, it will occur when both the trigger arm and the external arm signals are active.
[A] command complete	each time an A command has been completed.
measurement complete	after the module has completed sampling the data.
record complete	each time a complete record has been taken (see the Collect command).
triggered	when the module has been triggered, or each time the module has been triggered in the record mode. If the record mode has been programmed, a triggered or record complete interrupt may be 'lost' if an additional record was automatically taken prior to reading the interrupt from the previous record.

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The interrupt on Analyze (A) command complete is provided because many of the Analyze commands can take a relatively long time to complete. The BC command should be issued once before issuing any A command to enable this interrupt. Then each time an A command has been completed, an interrupt will be generated. Using the BC command does not preclude the use of any other interrupts. For example, if the measurement complete interrupt were programmed, once it becomes valid, an interrupt would be generated. Issuing a "BC;AA<LF>" command would then generate an interrupt when the average value has been calculated.

The READ STB VXI command can be used to determine the status of these signals when the interrupt occurred. The data returned in the status byte is as follows. A 0 in the bit position = true, and 1 = false, except as noted. If no interrupts are enabled (or active), the READ STB command will respond with an ASCII "30".

Bit	Meaning
0	measurement complete
1	triggered
2	armed
3	Analyze command complete
4,5	high (not used)
6	SRQ request (1 = true; 0 = false)
7	Record complete

Examples:

BT — generate an interrupt when the module is triggered. The READ STB command will respond with an ASCII "F9".

BA — generate an interrupt when the module is armed. The READ STB command will respond with an ASCII "FB".

BD — disable the interrupt.

B or BM — generate an interrupt when the measurement is complete. The READ STB command will respond with an ASCII "7C".

BR — generate an interrupt each time a complete record has been taken. The READ STB command will respond with an ASCII "79".

BC — generate an interrupt each time an Analyze command is complete. The READ STB command response will vary based on the conditions that were active when the command was issued. However, bit 3 will always be low for this condition.

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Command: C (Collect)

Syntax: C[x][y]

Purpose: The C command specifies the relative location of the trigger event in memory by controlling the number of samples taken prior to or after the trigger event.

Description: [x] specifies the data collection mode relative to the trigger, and can be any one of the following:

[x]	Definition
C	Center-trigger
F	Free-run
P	Pre-trigger (saves data prior to the trigger)
T	Post-trigger (default) (saves data following the trigger)
R[a]/[b]	Record mode

If [x] is not specified, the card will collect [y] samples following the trigger.

[y] is an optional decimal integer (from 4 to the total RAM size), which controls the number of samples taken relative to the trigger (address 0) for the pre- and post-trigger modes. The total RAM size depends on the option ordered:

262144 words	(256K)	Standard board
524288 words	(512K)	512K memory option
1048576 words	(1Mbyte)	1M memory option

If [y] is not specified, it defaults to (RAMsize - 100) for the post-trigger mode, and to 100 for the pre-trigger mode. If [y] is less than 4 or greater than RAMsize, an error is generated. For the center trigger mode, [y]'s equivalent is set to (RAMsize/2). [y] is ignored if specified for the center or free run modes.

The Collect command locates the trigger event in memory by controlling the number of samples taken prior to or after the trigger event. For the pre-trigger mode, [y] specifies the number of samples to be taken after the trigger occurs (address 0). The trigger event is thus located to see what occurred (RAMsize - [y]) samples before it, and [y] samples after it.

For the center-trigger mode, the trigger event (address 0) is "centered" in memory so that (RAMsize/2) samples are stored both before and after the trigger.

For the post-trigger mode, [y] specifies the number of samples to be taken prior to the trigger event (address 0). The trigger event is then located to see what occurred [y] samples prior to it, and (RAMsize - [y]) samples after it.

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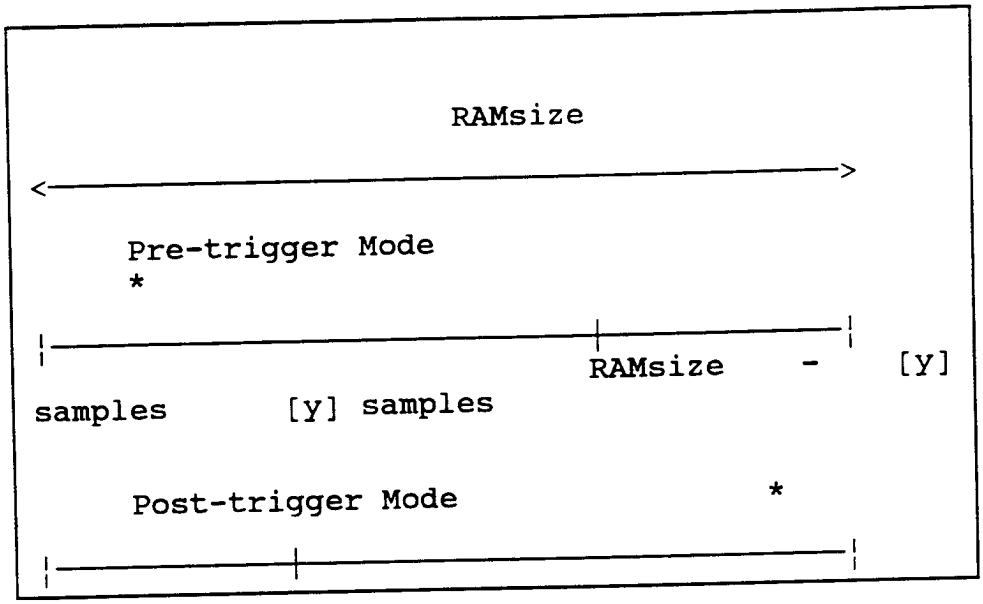

Figure 5: Collect Modes

Assuming 256K (262144 words) of memory, note that CP131072, CC, and CT131072 are all equivalent.

For the free run mode, data collection begins on receipt of the Trigger command, and will continue indefinitely until an Analyze (A), Greatest Value (G), Input (I), or Reset (R) command is received to stop the sampling. The trigger event (address 0) is the location where sampling stopped.

The Record mode allows memory to be sub-divided into individual records. For this mode, [a] is the record size, followed by an ASCII "/", followed by the total number of records to be taken, [b]. Once the Trigger command has been issued, each trigger event will collect [a] samples (1 minimum), until a total of [b] records (65534 maximum) has been taken. The Record mode collects only data taken after the trigger event (post-trigger). Each time a complete record has been taken, the trigger is rearmed. If a delay has been programmed (D command), it is also reloaded after each trigger event.

If (record size * number of records) is greater than (RAMsize - 2), an error will be generated. If [a] is not specified, it defaults to [b] records of [(RAMsize - 2)/b] samples each. If [b] is not specified, it defaults to [(RAMsize - 2)/a] records (65534 maximum) of [a] samples each. If neither [a] or [b] is specified, the default is one record of (RAMsize - 2) samples each. For example, CR1000 will collect 262 records [INTEGER (262142/ 1000)] of 1000 samples each.

To find the number of complete records taken at any time, use the Update Record Count (UC) command.

Examples: The following examples assume 256K of memory (262144 words).

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C1000 collect 1000 samples after the trigger event.

CC (center-trigger) collects 131072 (RAMsize/2) samples before and 131072 (RAMsize/2) samples after the trigger event, thus centering the trigger event in memory.

CF (free-run) collects data independently from any trigger event. Data collection stops on an Input Request command (I), a Greatest Value command (G), or an Analyze command (A).

CP (pre-trigger) stops data collection based on the trigger event, so that 262044 (RAMsize - 100) samples are collected before the trigger event, and 100 samples after the trigger event.

CP200 collects 261944 (RAMsize - 200) samples before the trigger event and 200 samples after the trigger event.

CT (post-trigger) stops data collection when 262044 (RAMsize - 100) samples have been collected after the trigger event. 100 samples will be saved before the trigger event.

CT500 collects 500 samples before the trigger event and 261644 (RAMsize - 500) samples after the trigger event.

CR1000/50
collects 50 records of 1000 samples each (50,000 samples total).

Note that the number of samples collected depends on when the T (Trigger arm) command is received, when the trigger occurs, and what the sampling rate is. The VX4240 Module begins sampling data following receipt of the T command. If the trigger is already active when the T command is executed, then less data may be collected than expected. For example, if the pre-trigger mode is specified, and the trigger is active when the T command is executed, then only data after the trigger will be collected (only 100 samples for the default value of [y]).

In addition, the time needed to initially fill the VX4240 Module's memory after receiving the T command is the RAMsize times the sampling rate. At a slower sampling rate (and assuming 262144 bytes of memory), for example, 25 µs/sample, this time is 262144 x 25 µs, or approximately 6.544 seconds. Therefore, an additional 6.544 seconds must be allowed after the trigger to completely fill the memory.

See the Trigger (T) command description, which has several options for precluding these conditions.

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NOTE: Because the memory is recirculating, there is a transition point between the oldest and the most recent data stored in memory. The transition point is the point where sampling stops. For example, for CP100, this point will be at address 100. Excluding this transition value in data analysis will prevent any possible misinterpretation of the signal.

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Command: D (Delay)

Syntax: D[x][y]

Purpose: The D command specifies the time delay or sample delay between the trigger event and the time that the data collection begins.

Description: The delay command is valid only for the Post-trigger and Record modes (see the C command), and is ignored if specified in any other mode.

[x] a single letter, T or S, that specifies what is being delayed:
T = delay time (default)
S = delay samples (delays [y] number of sample clocks)

[y] a real number (fixed or floating point) that specifies the delay:

[y]	Delay
0.0	No delay (default)
0 to 420 seconds	Delay time (in 200 ns increments)
0 to 2.0e9	Delay samples

If [y] is greater than 420 seconds for delay time, or greater than 2.0e9 for delay sample, then an error is generated. If [x] is not specified, delay time is assumed. If [y] is not specified, the delay value will be set to zero. If the specified time delay is not divisible by 200 ns, the delay is rounded down to the nearest divisible increment The Operational Setup (O) command can be used to view the actual value programmed.

For the delay time mode, data collection will begin after the specified amount of time has elapsed relative to the trigger. For the delay sample mode, data collection begins after the specified number of sample clocks have elapsed relative to the trigger. For example, if DS100 was programmed and the sampling frequency was 1 MHz (1 µs period), data collection would begin 100 x $1e^{-6}$ = 100 µs after the trigger event. If delay sample is programmed, the delay clocks are inhibited from counting if the external gate signal is active.

The last delay value programmed will remain in effect until a new delay value is programmed or the module is reset.

Examples:

D0.0	(or simply D) specifies no delay.
D150E-6	specifies a 150 µs delay.
D0.032767	specifies a 32.767-ms delay.
DT100	specifies a 100 second time delay.
DS40	specifies a 40 sample clock delay.
DS1E6	specifies a 1,000,000 sample clock delay.
D1.5E-6	is rounded down to a 1.4 µs delay.

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Command: E (Error)

Syntax: E[x]

Purpose: The E command is used to examine error conditions.

NOTE: This command must be issued by itself, and not as part of a command string.

Description: [x] can be either of the following letters:

[x]	Definition
A	An ASCII error message is returned.
N	The numeric value of the error code is returned.
Not specified	Defaults to N.

Input requests immediately following this command return the error information. The front panel display will show "E-xx", where xx is the error number.

Issuing this command and reading the error information clears the error and the front panel display. Since all commands are ignored following an error condition, only the first error is recorded and returned. The Error command is most useful during the initial program development. The error codes and the corresponding messages for all error conditions are listed below.

Response Syntax:

Command	Response
EA	THRESHOLD VALUE EXCEEDS THE VOLTAGE RANGE<CR><LF>
EN	08<CR><LF>

Error Codes: The error codes and corresponding error messages which may be returned by the VX4240 Module are as follows. Except where noted, all numbers are in decimal. All addresses, output data, and read-back data are in hexadecimal notation.

Error Code	Error Message
00	NO ERRORS
01	LCA LOAD FAILURE The programmable logic array failed to load correctly (U68).
02	CPU RAM FAILURE (Uxxx) ADDR yyyyyyyy: OUT zz IN ww Where xxx is the U number of the suspected chip, yyyyyyyy is the address where it failed, zz is the data output, and ww is the data read back.
03	COMMAND STRING EXCEEDS 160 TES

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04 BOARD NOT CALIBRATED

05 INVALID COMMAND 'x'
Where x is the first letter of the invalid command.

06 NUMBER ABOVE MAXIMUM FOR 'x' COMMAND
Where x is the first letter of the invalid command. The programmed parameter exceeds the maximum allowed value for the command.

07 NUMBER BELOW MINIMUM FOR 'x' COMMAND
Where x is the first letter of the invalid command. The programmed parameter is less than the minimum allowed value for the command.

08 THRESHOLD VALUE EXCEEDS THE VOLTAGE RANGE
A threshold was programmed (M command) which exceeds the voltage range.

09 COMMAND NOT IMPLEMENTED 'x'
Where x is the non-implemented command option.

10 IMPROPER COMMAND TERMINATION 'x'
Where 'x' is the command being processed when the error occurred.

11 RESERVED

12 (NUMBER OF RECORDS * RECORD SIZE) EXCEEDS MEMORY LIMIT

13 RESERVED

14 CONVERSION ERROR, NO NUMBER FOUND 'x'
Where x is the first letter of the invalid command.

15 CONVERSION ERROR, INVALID ARGUMENTS 'x'
Where x is the first letter of the invalid command.

16 CONVERSION ERROR, OUT OF RANGE 'x'
Where x is the first letter of the invalid command.

17 CALIBRATION ERROR, CANNOT ADJUST RANGE xxx OFFSET
Where xxx is the voltage range being adjusted. The digital to analog converter was unable to adjust the offset out of the input signal.

18 CALIBRATION ERROR, CANNOT ADJUST RANGE xxx GAIN
Where xxx is the voltage range being adjusted. The digital to analog converter was unable to adjust the gain for the input voltage applied and the range being calibrated.

19 OFFSET FAILURE - RANGE xxx (VALUE y.yyyyyyyE+yyy)
An offset failure was detected. xxx is the voltage range being tested, and y.yyyyyyyE+yyy is the value calculated.

20 GAIN FAILURE - RANGE xxx (VALUE y.yyyyyyyE+yyy)
A gain failure was detected. xxx is the voltage range being tested and y.yyyyyyyE+yyy is the value calculated.

21 NON-VOLATILE MEMORY FAILURE (Uxxx) OUTyyyy IN zzzz
Where xxx is the U number of the suspected chip, yyyy is the data loaded, and zzzz is the data read back.

22 HIGH SPEED RAM FAILURE ADDR yyyyyyyy: OUT zzzz IN wwww
Where yyyyyyyy is the address where the failure occurred, zzzz is the data output, and wwww is the data read back.

23 RESERVED

24 ADDRESS READBACK FAILURE (U02/U22) OUT xxxxxxxx IN yyyyyyyy
Where xxxxxxxx is the address loaded, and yyyyyyyy is the address read back.

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25 ADDRESS COUNTER FAILURE (Uxxx) OUT yyyyyyyy IN zzzzzzzz
Where xxx is the U number of the suspected chip, yyyyyyyy is the address loaded, and zzzzzzzz is the address read back.

26 THRESHOLD COMPARATOR FAILURE (Uxxx) OUT yyyy IN zzzz
Where xxx is the U number of the suspected chip, yyyy is the data output, and zzzz is the data read back.

27 DATA EXTENSION FAILURE (U431/U631) OUT yyyyyyyy IN zzzzzzzz
Where yyyyyyyy is the data output, and zzzzzzzz is the data read back.

28 RESERVED

29 RECORD MODE READBACK FAILURE (U42/U71) OUT yyyyy IN zzzzz
Where yyyyy is the number of records programmed, and zzzzz is the number of records taken, in decimal.

30 POSITIVE INPUT FAILURE (U120/K1201): VALUE = y.yyyyyyyy E+yyy
Where y.yyyyyyyyE+yyy is the value calculated, which S/B within 5% of 10 volts.

31 NEGATIVE INPUT FAILURE (K1401): VALUE = y.yyyyyyyyE+yyy
Where y.yyyyyyyyE+yyy is the value calculated, which S/B within 5% of -10 volts.

32 DIFFERENTIAL (CMRR) INPUT ERROR (VALUE = y.yyyyyyyyE+yyy)
Where y.yyyyyyyyE+yyy is the value calculated, which S/B within ±500 mV.

33 AC COUPLING FAILURE (K1501): VALUE = y.yyyyyyyyE+yyy
Where y.yyyyyyyyE+yyy is the value calculated, which S/B within ±50 mV.

34 SAMPLE COUNTER FAILURE (Uxxx) COUNT yyyyy SAMPLES zzzzz
Where xxx is the U number of the suspected chip, yyyyy is the number of counts programmed, and zzzzz is the actual number of counts read, in decimal.

35 RESERVED

36 MEASUREMENT COMPLETE STATUS BIT NOT ACTIVE (Uxxx)
Where xxx is the U number of the status readback latch.

37 ARMED STATUS BIT NOT ACTIVE (Uxxx)
Where xxx is the U number of the status readback latch.

38 TRIGGERED STATUS BIT NOT ACTIVE (Uxxx)
Where xxx is the U number of the status readback latch.

39 DONE STATUS BIT NOT ACTIVE (Uxxx)
Where xxx is the U number of the status readback latch.

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Command: F (Frequency) and P (Period)

Syntax:
F[x][y]
P[x][y]

Purpose: The F and P commands are interchangeable; they specify the frequency or sampling period (frequency = 1/period).

Description: [x] a single letter which specifies the source of the sample clock:

I	Internal (on-board) clock
V	VXI 10 MHz ECL backplane clock
E	External clock
not specified	defaults to I (Internal).

[y] a fixed or floating point number which specifies the frequency in Hertz, or period in seconds, in one of the following ranges:

10 MHz to 0.005 Hz (frequency)
100 ns to 200 seconds (period) in 100 ns increments.

All values are rounded down to the nearest period value increment (or up to the nearest frequency range). The Operational Setup (O) command can be used to view the actual value programmed. For the external clock, the frequency is left unchanged. If [y] is not specified, an error is generated.

Examples:

P100E-9	specifies a period of 100 ns (10 MHz).
FI10	specifies a sampling frequency of 10 Hz.
F20E+3	specifies a frequency of 20 kHz (50 ms).
FV1.234E6	specifies a frequency of 1.25 MHz using the VXIbus clock as the reference (rounded up to the nearest frequency range).
PE125E-9	specifies an external clock with a period of 125ns (8MHz).
P250E-9	specifies a period of 200 ns (5 MHz) (rounded down to the nearest period increment).

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Command: G (Greatest/Least value)

Syntax: G[x]

Purpose: The G command reports the greatest or least value seen for the programmed voltage range since the last trigger event.

Description: [x] a single letter, G or L, which specifies:

G	reports the greatest value seen since the last trigger.
L	reports the least value seen since the last trigger.
not specified	the greatest value will be returned.

If a threshold trigger is programmed, the G command returns the threshold value if the trigger event has not occurred.

If the Record mode is specified (C command) with a threshold trigger (M command), the G command returns the threshold value (the maximums and minimums are not updated). The G command reports values based on the eight most significant bits in the data only. See the Mode (M) command for a more detailed discussion of the G command's operation.

Issuing a G command immediately halts any data collection in process. Input requests immediately following this command return the value.

Example:

Command	Response
GG	GV = _+1.00000E+000<CR><LF>
GL	LV = _-1.00000E+000<CR><LF>

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Command: I (Input request)

Syntax: I[x][y][f][Sz]
IR[n]/[x][y][f][Sz]

Purpose: The I command specifies the address control, the address (relative to the trigger), and the format for data reporting.

Description: [x] the address control, can be one of the following:

[x]	Definition
D	Automatic decrement to the next address
I	Automatic increment to the next address
Not specified	Defaults to I

[y] the address relative to the trigger, can be one of the following:

[y]	Definition
+0 to +RAMsize*	Positive offset from trigger (or start of the record)
-0 to -RAMsize*	Negative offset from trigger (or start of the record)
Not specified	Defaults to +0

* RAMsize = 262144 for 256K, 524288 for 512K, or 1048576 for 1MB.

[f] the data reporting format, can be one of the following:

[f]	Definition
A	ASCII transfer
B	Offset binary transfer
K[b]	ASCII block transfer, where [b] is the block size (1 to 2500). The data values will be separated with the delimiter defined by the L command.
T	Two's-complement, binary transfer
Not specified	Defaults to A

[n] the record number.

Input requests immediately following this command return the data. Additional input requests automatically address and output the data for the next appropriate location. An I command immediately stops any data collection in process.

[Sz] optional parameter specifying a step size; where [Sz] = 1 to 65536. If [Sz] is not specified, it defaults to 1.

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ASCII Transfer

Data is automatically scaled for ASCII transfers, based on the programmed input range, and reported as twelve ASCII characters followed by <CR><LF> in the following format:

Sxxx.xxxxxxx<CR><LF>

where:	S	=	+ or -
	x	=	Decimal digit (0-9)
	.	=	Decimal point
	<CR>	=	Carriage return
	<LF>	=	Line feed

Example: +012.2378910<CR><LF> or -100.1234567<CR><LF>

Binary Transfer

If a binary transfer is specified, then the data is reported as two bytes of binary data per data value, with no <CR><LF> characters in between or at the end of the transfer. For offset binary transfers, hexadecimal 0000 represents negative full scale, hexadecimal 8000 represents 0, and hexadecimal FFFF represents positive full scale. For two's-complement binary transfers, hexadecimal 8000 represents negative full scale, hexadecimal 0000 represents 0, and hexadecimal 7FFF represents positive full scale. A binary transfer is terminated by issuing a new command to the module. **Refer to *Appendix J: Binary Transfer* if you are using a National Instruments GPIB-VXI/C Slot 0 module.**

ASCII Block Transfer

For ASCII block transfers, <CR><LF> characters are inserted only at the end of a block, and each value in the block is separated by a semicolon (;), or the optionally defined delimiter specified by the L command.

Step Option

The step option can be used for data de-multiplexing. If specified, the data values returned are offset the specified number of locations from each other. For example, 'I0K4S4' returns the data in locations 0, 4, 8, and 12. There is a negligible time difference when specifying a step size for ASCII transfers. For maximum binary transfer rates, the step option should not be used. This process allows direct memory access to the card's data. If a step is specified, the binary transfer rate will decrease, because the CPU must reload the address after each transfer.

Examples:

II+0A (or simply I) specifies an ASCII transfer with auto-increment and an offset of +0. Input requests following this command return the data in the ASCII format, starting with the data at the trigger event (address 0). This is the default mode.

ID-10A specifies an ASCII transfer with auto-decrement starting 10 samples before the trigger event. The input requests following this command return the data in ASCII format.

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II-5K10 reports ten values (including the trigger value), in the ASCII block format starting five samples before the trigger event and ending four samples after the trigger event.

ID10K5 reports five values in the ASCII block format starting ten samples after the trigger event. The command is: input, auto-decrement, start 10 locations after the trigger event, and return 5 ASCII values in a block, for example:

-001.2960000;+000.0320000;+000.7840000;+001.0240000;+001.7041111;<CR><LF>

IR47K100 returns the first 100 values of record 47. If record 47 does not exist, an error will be generated. Data is reported beginning at the first location of record 47.

IR3/100 returns the value stored at the 100th location of record 3.

IB,IT returns two bytes of binary data for each value, starting at the trigger address. The first input returns the most significant byte. The second input returns the least significant nibble in bit positions 7, 6, 5, and 4 (LSB). Bits 0 to 3 will be zero.

Input 1 -	MXXXXXXX	where M is the MSB
Input 2 -	XXXL0000	where L is the LSB

If the data value was 73C hex (0111 0011 1100 binary), the most significant byte (73h or 0111 0011 binary) would be followed by the least significant left-justified byte (C0h or 1100 0000 binary). If the data was sampled on the 1 volt range (per bit value = 488.2812 µV), this value is equivalent to:

<u>two's complement binary</u>:
73Ch = +1852 counts ≡ 1852 * perbit value = +904.3 mV
73C0h = +29632 counts ≡ 29632 * (perbit/16) = +904.3 mV

<u>offset binary</u>:
73Ch = -196 counts ≡ -196 * perbit value = -0.09570
73C0h = -3136 counts ≡ -3136 * (perbit/16) = -0.09570

I0S4 returns every fourth data value, beginning at address 0.

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Command: J (Math Operations)

Syntax: Jz[x]/[y]

Purpose: The J command allows the VX4240 to be used as a calculator to perform arithmetic operations.

Description: z is a single letter which specifies the type of function to be calculated.

[x] and [y] are one or more variables, whose meaning depends on the function chosen. For the commands below, [x] and [y] must be in a valid numeric format, as described at the beginning of the Operation section. Variables and arithmetic operations are not permitted for the command arguments. All responses are of the format:

±x.xxxxxxxe±xxx<CR><LF>

where x is a decimal digit 0 through 9.

Command	Function	Note
JC[x]	cosine	[x] is an angle in radians
JE[x]	exponential (base e)	$e^{[x]}$
JF[x]	hyperbolic sine	[x] is an angle in radians
JG[x]	hyperbolic cosine	[x] is an angle in radians
JH[x]	hyperbolic tangent	[x] is an angle in radians
JJ[x]	floor	rounds [x] down to the nearest integer (5.23 is rounded to 5.00)
JK[x]	round	rounds [x] up to the nearest integer (5.23 is rounded to 6.00)
JL[x]	log base 10	log [x]
JM[x]/[y]	mod [x][y]	returns the fractional part of [x]/[y] (returns the remainder for a division)
JN[x]	natural log (base e)	ln [x]

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JP[x]	arc sine	returns the angle whose sine is equal to [x] radians. Results are in the range -pi/2 to pi/2.
JQ[x]	arc cosine	returns the angle whose cosine is equal to [x] radians. Results are in the range 0 to pi.
JR[x]	arc tangent	returns the angle whose tangent is equal to [x] radians. Numbers are chosen between -pi/2 and pi/2.
JS[x]	sine	[x] is an angle in radians
JT[x]	tangent	[x] is an angle in radians
JX[x]/[y]	exponential (any base)	$[x]^{[y]}$

Examples:

Command	Response
JL20	+1.3010300E+000<CR><LF>
JX10/1.30103	+2.0000000E+001<CR><LF>
JM5/3	+6.6666669E-001<CR><LF>
JJ-17.43	-1.8000000E+001<CR><LF>

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Command: K (Calibrate)

Syntax: K[x]

Purpose: The K command is used to calibrate the gain and offset parameters of the module, or for software calibration during operation.

Description:

[x]	Definition
An	calibrate the AC gain, where n = 5 or 50
G(range)	calibrate the gain
O(range)	calibrate the offset
S(range)	calibrate both the gain and offset
X	load RAM with a ramp
Zn	calibrate the differential gain, where n = 0.5 or 5
(range)	returns the calculated offset voltage

(range) = 0.5, 1, 2, 5, 10, 20, 50, or 100.

If (range) is incorrectly specified for the KS, KG, and KO commands, an error will be generated.

The KA command is used to adjust the AC gain of the upper ranges (as defined in the Calibration Procedure section in the Service Manual). The module will return the RMS voltage on completion. While the KA command is being executed, the front panel display will be flashing hex values. Issuing a read to the module will exit it from the command loop, will return the data, and will display "RDY".

The KG command performs an automatic gain adjustment for the specified input range (as defined in the Calibration Procedure section in the Service Manual). The module will return the calibrated voltage value on completion. While the KG command is being executed, the character display will be flashing hex values, and will display "RDY" when the command is complete. The KG command can take several minutes to complete.

The KO command performs an automatic offset calibration for the input range specified (as defined in the Calibration Procedure section in the Service Manual). The module will return the calibrated offset value when finished. While the KO command is being executed, the character display will be flashing hex values, and will display "RDY" when the command is complete. The KO command can take several minutes to complete.

The KS command performs the equivalent of a KO and a KG command and returns both the offset and gain values on completion. For the KS, KG, and KO commands, the calibrated values are automatically stored in non-volatile memory for recall during operation. If the module can not be calibrated, an error is generated for these commands.

The KX command is used for debugging when operation of the memory is suspect. Issuing this command loads the data memory with a ramp (offset 16)

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(0000,0010,0020,...FFF0,0000...) for subsequent readback verification. No data is returned by this command.

The KZ command is used to adjust the differential gain of the input circuit (as defined in the Calibration Procedure section). The module will return the differential voltage on completion. While the command is being executed, the front panel display will be flashing hex values. Issuing a read to the module will exit it from the command loop, will return the data, and will display "RDY".

The K (range) command may be used for software calibration during operation. By taking an offset reading at the voltage range of interest, the offset can be compensated for in subsequent measurements by subtracting the offset reading from the measurement value to get a more accurate measurement value. This technique can be used to compensate for long term drift or temperature drift. This command returns the offset voltage, but does not save the value in non-volatile memory.

Examples:

Command	Response
KS1	KS=_+0.0000000E+000_(0129)_+9.8001099E-001_(3408)<CR><LF> The first value is the offset, the second value is the gain voltage, and the numbers in parentheses are the corresponding internal DAC load values.
KG2	KG=_+1.9599609E+000<CR><LF> The value is the calculated gain voltage.
KO5	KO=_-1.5258789E-004<CR><LF> The value is the calculated offset.
KX	Loads RAM with a ramp; no data is returned.
K20	KV=_-5.4931641E-003<CR><LF> The value is the calculated offset voltage.
KZ5	KD=_+3.7819824E-002<CR><LF> The value returned is the calculated common mode RMS voltage.
KA5	KA=_+3.4602302E+000<CR><LF> The value returned is the calculated RMS voltage.

(_ indicates an ASCII space character)

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Command: L (Define Delimiter)

Syntax: L[x]

Purpose: This command defines the delimiting character to be used between data values of large data blocks.

Description: [x] is one of the following:

[x]	Delimiter	ASCII
S	Space character	20h
C	Comma	2Ch
0	Null	00h
N	Semi-colon	3Bh

Not specified - defaults to N

The L command allows changing the data value delimiters when large data blocks are being transferred, to optimize software for the language being used. Once an L command has been issued, all data blocks are delimited with the specified character. The affected commands are:

- any A command issued with the [H] parameter
- AD, AC, AQ, and AH commands
- I (Input) command with the block (K) option
- O (operational setup) command

Examples:

LS defines the delimiter as an ASCII space character.

L0 defines the delimiter as an ASCII null character (00 hex).

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Command: M (Trigger Mode)

Syntax: M[x][y][z]

Purpose: The M command specifies the trigger condition which starts data collection following a T command.

Description: [x] and [z] can be any one of the following:

[x,z]	Definition
A[w]	Software trigger; module begins digitizing on T command (default).
C[w]	VXI command trigger.
E+[w]	External trigger, positive, TTL edge.
E-[w]	External trigger negative, TTL edge.
N±0 to ±100[w]	Negative threshold trigger, level in volts (e.g., N+10.250).
P±0 to ±100[w]	Positive threshold trigger, level in volts (e.g., P+10.250).
±S±0 to 100[w]	Slope trigger with threshhold.
Va[w]	VXIbus hardware trigger: a = 0 to 7, Input TTL trigger select.

[w] optionally allows specifying a VXIbus output TTL trigger. The format is /w, where w = 0 to 7, output trigger select.

[y] an optional operator which allows any two trigger conditions to be logically ANDed or ORd:

[y]	Specifies
#	OR the [x] and [z] trigger conditions
&	AND the [x] and [z] trigger conditions

If [y] is not specified, the trigger is ORd with itself (single trigger condition).

For the software trigger (MA), the module will begin digitizing on receipt of the Trigger (T) command. For the VXI Trigger command, the module begins digitizing on receipt of the VXIbus word serial Trigger command. For the external triggers (E+ and E-), the module begins digitizing when the programmed edge is seen. For example, if ME+ was programmed and the signal was high, the module would not trigger until the signal went low and then back high. For the VXIbus TTL triggers (TTLTRG0 - TTLTRG7), the module begins digitizing when the programmed trigger edge is seen. See the W command for information on specifying the active trigger edge for the VXI TTL trigger.

For a threshold trigger, the VX4240 Module begins digitizing when the input voltage is greater than the programmed threshold for the MP command, or when the input voltage is less than the programmed threshold for the MN command. The threshold value may be positive or negative for both cases. If a threshold level is defined outside the voltage range, an error is generated when the T command is received.

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For the slope trigger, the module begins digitizing one sample clock after the specified threshhold is exceeded with the specified slope. This allows triggering the module at a threshhold value in any quadrant of the signal.

The actual threshold value is based on the per-bit value of the range programmed, and rounded to the nearest increment. The per-bit values are given in the Specifications section of this manual under Resolution. Only the most significant eight bits of resolution are used for the thresholds. The operational setup (O) command can be used to view the actual values programmed.

NOTE: Two comparators are used to monitor the incoming signal. Once triggered, the first comparator is updated every time the data exceeds the previous value. The second comparator is updated every time the data is less than the previous value. These values can be read using the G command. The comparators are not updated if the module is programmed in the Record mode. If a threshold trigger is not programmed, the comparators will be loaded with (- full scale) and (+ full scale) respectively. The comparators are inhibited if the external gate signal is active.

When specifying the "AND" of two trigger conditions, the conditions are asynchronous with respect to each other. That is, once one condition is satisfied, it is latched internally. Then, when the second condition is satisfied, the module is triggered. However, for a threshhold or slope trigger, the threshhold/slope trigger is not activated until after the other trigger condition has occurred.

If both a VXIbus input trigger and VXIbus output trigger ([w] option) are specified, it is recommended they be specified on different lines to protect against loss of the output trigger. This could happen, for example, if the input trigger line was still active (still low) when the VX4240 Module triggers. Since the trigger lines are open-collector, driving the output trigger low would have no effect, since the signal is already low, and the trigger out would be lost.

Examples:

ME+	specifies a positive edge external trigger.
MA	specifies a software trigger. The module will trigger when the T command is received.
MP9.5#E-	specifies either a +9.5 volt threshold or a negative edge external trigger.
MP9.5&P9.7	specifies that comparator 1 must be >9.5 volts, and comparator 2 must be >9.7 volts. Once triggered, the first comparator will save the maximum voltage above 9.5 volts, and the second comparator will save the minimum below 9.7 volts.
MN9.5&N9.3	is the same as the previous example, except that it looks for voltages that go below the programmed level.

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MP1#N-1	is a "window" trigger. The module will trigger if the voltage goes outside ±1 volt.
M+S+5	Trigger on a positive slope, 5 Volt threshhold (1st quadrant).
M+S-3	Trigger on a positive slope, -3 Volt threshhold (4th quadrant).
M-S+1.7	Trigger on a negative slope, +1.7 Volt threshhold (2nd quadrant).
M-S-2.4	Trigger on a negative slope, -2.3 Volt threshhold (3rd quadrant).
MV0/7#C	specifies triggering on the VXIbus TTLTRG0 or on the VXI TRIGGER command. TTLTRG7 will be strobed when the module is triggered.
ME-/0	specifies a negative edge, external trigger. TTLTRG0 of the VXI bus will be strobed when the module is triggered.

NOTE: When defining multiple triggers, be careful not to define impossible conditions. For example, ME+&E- is an invalid trigger condition because the two conditions are mutually exclusive. Similarly, MP+1&N-1 is invalid, because the voltage can not be greater than +1 and less than -1 at the same time.

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Command: N (fft summation method)

Syntax: N[x]

Purpose: The N command can be used to select the method used by the FFT built-in processing routines to determine the peaks of the spectrum. The default is to use a three cell summation as described in Appendix E.

[x] can be any one of the following:

1	Disable 3-cell summation
0	Enable 3-cell summation (default).

The N command allows selecting the optimal processing methods for determining the amplitudes of the frequency components. For signals (and harmonics) closely lined with the FFT frequency cells, N1 should be used. This requires careful selection of the FFT size and sampling frequency to match the input signal. For general purpose applications, the default N) should be used.

Examples:

N1	disable 3-cell summation
N0	enable 3-cell summation

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Command: O (Operational setup)

Syntax: O

Purpose: The O command returns the operational setup parameters for the VX4240 Module.

Description: The information returned by the O command will reflect the programmed setup parameters. The front panel display may not agree with this, if the T (Trigger) command has not yet put the programmed parameters into effect.

The information returned is in the following format. _ indicates an ASCII space character. If an optional delimiter has been specified with the L command, all semicolons will be replaced with that delimiter.

MODE_[A]_[B]_[C];_COLLECT_[D]_[E]_RECORDS_[F];_LEVEL1
_[G];_LEVEL2_[H];_VOLTAGE_[I];_PERBIT_[K];_INPUT_[L]
OHMS[M]_[J]_[MM];_FREQ_[N];_PER_[O];_CLKSRC_[P];
DELAY[Q]_[R];_INTERRUPT_[S];_RAMSIZE_[T];_EDGES_[U];
RTCLK[V];VXITO_[W];<CR><LF>

The meaning of each variable is as follows:

[A],[C]	TRGS	software (T command trigger)
	VXI[x]	VXI hardware trigger (TTLTRG0 - 7), where [x] is the input trigger number.
	VXIC	VXI command trigger
	EXT+	external, positive edge trigger
	EXT-	external, negative edge trigger
	THR+	positive (greater than) threshold trigger
	THR-	negative (less than) threshold trigger
	SLP+	positive slope trigger
	SLP-	negative slope trigger
[B]	&	logical AND of [A] and [C] triggers
	#	logical OR of [A] and [C] triggers
[D]	POST	post trigger collect mode
	PRET	pre-trigger collect mode
	CENT	center trigger collect mode
	FREE	free run trigger collect mode
	RECM	record mode collection
[E],[F]	XXXXXXX	integer number (0 to RAMsize) indicating the collect count and number of records to take (padded with leading zeros if required).

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[G],[H] ±X.XXXXXE±XXX
floating point number indicating the programmed threshold levels.

[I] ±X.XXE±XXX
the programmed voltage range.

[J] AC ac coupled input
DC dc coupled input

[K] X.XXXXXXE±XXX
perbit value of the data.

[L] 50 50 Ohm input load
1M 1 MOhm input load

[M] SING single ended input
DIFF differential input

[MM] CON connector (S3) input
BNC BNC input

[N],[O] X.XXXXXXXE±XXX
sampling frequency/period

[P] INT internal clock source
EXT external clock source
VXI VXI clock

[Q] TIME delay time
SAMP delay samples

[R] X.XXXXXXXXXE±XXX
time value or sample count

[S] ACP if interrupt on Analyze command complete programmed
MCP if interrupt on measurement complete programmed
TRG if interrupt on triggered programmed
ARM if interrupt on armed programmed
RCP if interrupt on new record complete programmed

If an interrupt is not programmed, the data displayed will be "DIS".

[T] XXXXXXX amount of data memory on the module.

[U] abcd programmed control line active edges (+ or -)
a corresponds to the VXI input trigger
b corresponds to the output trigger
c corresponds to the arm input
d corresponds to the arm output

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If no active edges are programmed, the value displayed will be a "-".

[V] XXXXXXX
number of sample clocks for every real time data update.

[W] 0 to 7 for the programmed VXI output TTL trigger, or "X" if no VXI output trigger is programmed.

The default operational response is:

MODE TRGS # TRGS; COLLECT POST 0262044 RECORDS 0000001; LEVEL1 +1.00000E+002; LEVEL2 -1.00000E+002; VOLTAGE 1.00E+002; PERBIT 4.882812E-002; INPUT 1M OHMS DIFF DC BNC; FREQ 1.0000000E+007; PER 1.0000000E-007; CLKSRC INT; DELAY TIME 0.000000000E+000; INTERRUPT DIS; RAMSIZE 0262144; EDGES ----; RTCLK 0000001; VXITO X;

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P[x] See F (Frequency) command for a description of the P[x] command.

Command: Q (Query status)

Syntax: Q[x]

Purpose: The Q command returns the current status of the VX4240 Module for the next input request to the module.

[x] can be any one of the following:

[x]	Definition
S	1 = Self test failed
	0 = Self test passed
E	1 = Programming error
	0 = No programming errors
P	1 = Measurement in progress
	0 = No measurement in progress
T	1 = Triggered
	0 = Not triggered
M	1 = Memory full
	0 = Memory not full
R	1 = Real time data updated
	0 = Real time data not updated
Not specified	The default lists the first five above conditions (preceded by S) in the order SEPTM. The default presents the current situation for each condition.

The Q command can request the status of a single condition, or the summary of all five individual conditions. Query the status of all five conditions by entering the default Q, or query any one of the conditions by entering QS, QE, QP, QT, QR, or QM. All responses to the command are preceded by the ASCII character S (unique to the status response).

Once a Q command is received, all subsequent input requests respond with the specified information until another input type command is received.

Response Syntax:

Q Response while the module is actively collecting data:

S00110<CR><LF>

This command response indicates that the self test was passed; that there are no programming errors; that the measurement is in progress; that it is triggered; and that the memory is not full.

QE Response after the module has been programmed and no programming errors were found:

S0<CR><LF>

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Command: R (Reset)

Syntax: R

Purpose: The R command resets the VX4240 Module to its default power-up state.

The default operational setup parameters are:

Mode: software trigger
Collect: Post-trigger, count = RAMsize - 100
Threshold Level 1: +100
Threshold Level 2: -100
Voltage: ±100V, dc coupled, 1 MOhm input impedance, single-ended BNC input
Frequency: 10 MHz, internal clock
Delay: 0
All interrupts disabled
All control I/O signals negative edge triggered
VXI output trigger disabled
Real time update frequency: 10 MHz (update every 1 sample clock)
Block delimiter: semi-colon

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Command: S (Self test)

Syntax: S

Purpose: The S command causes the VX4240 Module to execute a self test and return to its power-up state. The results of the self test can be obtained by issuing the Q (Query status) or E (Error) command.

The following tests are performed:

Character Display	Test	Error No.	Function
RAM	CPU RAM	2	loads 32770 bytes of CPU memory with an incrementing count, and then verifies that the data read back matches the data loaded.
NVRM	non-volatile memory	21	performs a write/read operation to verify the non-volatile memory
ACNT	high-speed address counters	24,25	this test first loads and then verifies via readback the A/D address counters (error 24). It then verifies each of the address counters by reading the address each time it is clocked, up to the total RAM size.
HRAM	high speed RAM	22	verifies all of the A/D memory in the same manner as the CPU RAM test.
THRL THRH	threshold comparators	26	verifies that the threshold comparators can be loaded and read back.
BEXT	bus extension latches	27	verifies the proper operation of the sign extend latches between A/D memory and the CPU.
STAT	status bits	37,38,40	verifies the armed, triggered, and LCA load complete status readback latches.
RECC	record counters	29,36	verifies the operation of the record mode counters (error 29). In addition, verifies the measurement complete status bit (error 36).
SCNT	sample counters	34	verifies the sample counters by ensuring that the number of samples taken equals the number programmed.

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analog front end:

HREF	30	verifies the high input signal path using the on-board voltage reference.
LREF	31	verifies the low input signal path.
CMRR	32	verifies the common mode (differential input) circuitry.
ACCP	33	verifies the AC coupling relays.
OXXX offset/gain GXXX values	19,20	verifies that the offset voltages for each range are less than ±5% of full scale. Using an internal voltage reference, verifies that the gain on ranges 1, 2, 10, 20, and 50 is within 5% of the ideal voltage. The ideal voltage is 0.213 volts for ranges 1 and 2, and 10 volts for ranges 10, 20, and 50. "XXX" is the range being tested.

The power-up self test is a subset of the commanded self test, to allow completion in five seconds. The differences are:

Test	Commanded	Power-up
CPU RAM	tests 32770 locations	tests 1000 locations
high speed address counters	tests all addresses	tests the first 1000 addresses
high speed RAM	tests all RAM	tests the first 4100 RAM locations
offset/gain	tests all ranges	tests range 1 only
record counters	tests for 65270 records	tests for 260 records

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Command: T (Trigger arm)

Syntax: T[x][y]

Purpose: The T command arms the trigger.

Description: [x] E, an optional parameter. If specified, it enables the external arm input. If [x] is not specified, the external arm input is ignored.

[y] a single letter, specifying:

[y]	specifies
A	arm trigger
D[z]	delay trigger; [z] is the optional delay count from 0 to RAMsize (defaults to RAMsize)
F	fast trigger
S	software trigger
not specified	performs the equivalent of a TA and TS command

If the external arm signal is programmed, the triggers will not be armed until both a trigger command is received and the external arm signal is valid. Be careful to ensure that a trigger is not lost when using the external arm, since the triggers are not armed until the external arm signal is active. See the W command for information on programming the active edge of the arm signal.

Trigger arming normally follows this sequence:

1) Data memory is cleared.

2) Hardware is set up, based on previously loaded commands or their defaults.

3) VX4240 Module is armed.

4) Data collection begins following the T command as specified by the Trigger Mode command (see the M command).

These four steps are performed for the Trigger Arm (TA) command. If a software trigger has been programmed with the Mode (M) command, it is not executed. This allows arming the module, then using software to control when the board is triggered by issuing a TS command.

The TS command executes a software trigger. Steps 1 through 3 above are not performed unless the module is not armed (in which case it does all four steps). The TS command is most useful in the Record mode where it is desired to use software to control the taking of a new record.

The Trigger Delay (TD) command performs steps 2 through 4 above. However, after the card is armed, the triggers are not armed until enough time has elapsed

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to guarantee that memory is filled with valid data prior to arming the triggers. If [z] is specified, the delay period will be [z] times the sampling frequency. This allows controlling the number of samples taken prior to arming the trigger. For example, if CP10000;TD2000 was programmed and the trigger was active, the card would collect 2000 samples prior to the trigger and 10000 samples after it. During this delay period, the front panel display will read "WAIT".

The Trigger Fast (TF) command performs only steps 2 through 4 above, reducing the maximum trigger latency.

The Trigger (T) command is the normal mode of triggering the module. It performs the above four steps in addition to executing a software trigger (if programmed).

All future T commands repeat the appropriate sequence until the module is reset.

Examples:

T Arm the trigger(s) and execute a software trigger (if programmed).

TF The TF (Trigger Fast) command performs the same sequence as the T command, except that data memory is not cleared.

TEA Enable the external arm, and arm the trigger(s).

TD Delay arming the trigger until memory is filled with valid data.

TD1000
Delay arming the trigger until 1000 samples have been taken.

Approximate trigger command to trigger arming delays: [For AC coupling, add 500 ms to all the times except TS (armed).]

Command	Delay
T, TA	(3 sample clock periods) + (RAMsize * 2.25µs) + 10 ms
TD	(sampling period) * (memory size) * 1.1 + 10 ms
TF	(3 sample clock periods) + 10 ms
TS	(card not armed) same as the TA command
TS	(card armed) < 100 µs
TD1000	(sampling period) * (1000) + 10 ms

Assuming 256K of memory (262144), and a sampling frequency of 10 MHz (100 ns period), these delays are nominally:

TA = (3 * 100e-9) + (262144 + 2.25e-6) + 10e-3 = 599.824 ms

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TD = (100e-9 * 262144 * 1.1) + 10 ms = 38.84 ms

TF = (3 * 100 e-9) + 10 ms ≈ 10 ms

NOTE: The module actually begins sampling data 10 ms (relay switching delay) after receipt of the trigger command, but does not arm the trigger until after the trigger delay time described above (minus 10 ms) has elapsed. Then, once the trigger(s) has occurred, the number of samples specified by the Collect command are taken, and then sampling stops. The exceptions to this pattern are:

1) If programmed in the Record mode, sampling does not start until after the trigger(s) occur.

2) If programmed with a delay (D command), sampling does not start until after the trigger(s) occur and the programmed delay has elapsed.

3) If the External Arm is programmed, sampling does not start until the external arm is active, which then arms the trigger(s).

The diagram on the next page (abbreviated from Appendix D) shows the interrelationships between the Trigger (T), Delay (D), and Collect (C) commands.

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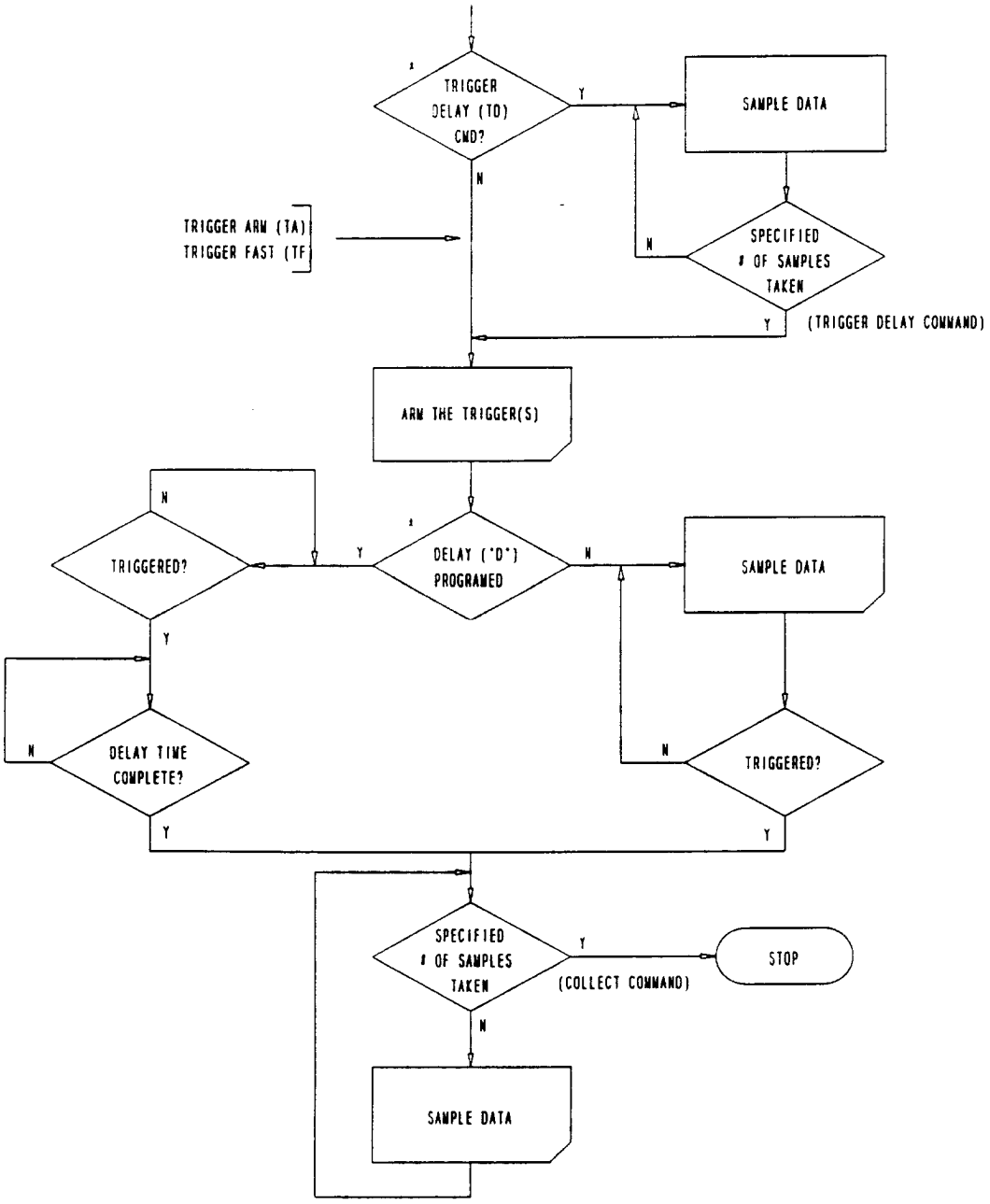

Figure 6: T, D, and C Command Relationships

* If a delay is programmed with the D command, the TD command will have no effect.

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Command: U (Update)

Syntax: U[x]

Purpose: The U command is used to read the number of complete records taken, to read the real time data, or to set up the real-time update count.

Description: [x] one of the following single letters, which specifies:

C reads the current record count (number of complete records taken), and returns information in the format RC=_xxxxx<CR><LF>.

F[n] real time update count, [n] = 1 to 8.3886E6 sample clocks.

R reads the real time data, and returns information in the format +x.xxxxxxxE+xxx<CR><LF>

B reads the real time data, and returns the value in twos complement binary (same format as the IT command).

If [x] is not specified, an error is generated.

The UC command reports the number of complete records taken at any time (see the CR command). The UF command controls how often the data is updated, and the UR command reports the sampled data value. If the UF command is not programmed, it defaults to UF1. The real time update function allows reading data in progress when the module is actively sampling.

Once a UR or UB command is received, all subsequent input requests respond with the specified information until another command is written to the card. If the real time data has not been updated, the value returned will be the last value updated. The QR command can be used to tell whether or not the data has been updated. The real time update clock is inhibited if the external gate signal is active.

Examples: The command UC could return

RC=_00001<CR><LF>

The command UR could return

+1.0000000E+001<CR><LF>

UF5 update real time data every 5 sample clocks.

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Command: V (Voltage range)

Syntax: V[w][x][y][z][bb]

Purpose: The V command specifies the input coupling and the voltage range. The voltage range setting includes a variable range setting capability.

Description: [w] a single letter, A or D, which specifies coupling:

A	ac coupling *
D	dc coupling
not specified	dc coupling

[x] specifies the voltage range, between 0.5 and 100 volts. The range value may be set at any value between these limits, and is not limited to standard range values. However, the module is calibrated at the following range values:

0.5	±0.5 volts
1	±1 volt
2	±2 volts
5	±5 volts
10	±10 volts
20	±20 volts
50	±50 volts
100	±100 volts (default)

Setting the range to a value other than the calibrated values improves the voltage resolution proportional to the decrease in range from the next higher calibrated range. Note that accuracy as a percent of reading may be slightly degraded, since the range is not at a calibrated value.

If [x] is less than 0.5 or greater than 100, an error is generated.

[y] a single letter, M or F, which specifies the input impedance:

M	1 MOhm input impedance
F	50 Ohm input impedance *
not specified	defaults to M

The 50 Ohm load is only valid for ranges 10 and below, and is ignored if specified for a higher range.

[z] a single letter, S or D, which specifies the input:

S	single ended input
D	differential input
not specified	defaults to S

**NOTE:* AC coupling and 50 Ohm input load are mutually exclusive. If both are specified, the 50 Ohm input will be ignored.

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[bb] a single letter, C or B, which specifies:

C	connector (DB25) signal inputs
B	BNC signal inputs
not specified	defaults to B

[y], [z], and [bb] may be programmed in any order.

Examples:

VD10	specifies a dc-coupled, ±10-volt range.
VA5	specifies an ac-coupled, ±5-volt range.
V1	specifies a dc-coupled, ±1-volt range.
V1.1FD	specifies a dc coupled, ±1.1 volt 50 Ohm, differential input.
VA100S	specifies an ac coupled, ±100 volt, 1 MOhm, single ended input.
V1SF	specifies a dc coupled, ±1 volt, 50 Ohm, single ended input.
VA1MDC	specifies an ac coupled, ±1 volt, 1 MOhm, differential input from the DB25 connector input.

NOTE: The LEDs on the front panel will reflect the currently programmed state. If the module is actively sampling data, however, the LEDs will not light until after the sampling has stopped.

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Command: W (Define control signal edges)

Syntax: W[x]

Purpose: The W command defines the active edges for the arm input, the arm output, the trigger output, and the VXI trigger in signals.

Description: [x] is optional, and specifies the signal and edge. [x] can be one or more of the following:

A[±]	external arm in edge
O[±]	arm out edge
T[±]	trigger out edge
V[±]	VXI input trigger edge

If a signal is not programmed, it remains in its previously defined state (or the default state of negative true). If the VXI triggers are not enabled (with the M command), the W command will have no effect on them. Note that the VXIbus input trigger edge is programmable, while the VXIbus output trigger is fixed at negative edge true. The arm out signal remains in its active state as long as the card is armed. The trigger out signal remains in its active state until the card is re-armed.

Examples: WA+O-T+ defines the arm in and trigger out signals as positive edge true, and the arm out signal as negative edge true.

WO+ defines the arm out signal as positive edge true.

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Command: Z (Version Level)

Syntax: Z

Purpose: The Z command returns the module number and the current software version level. The format of the response is:

TEK_VX4240_VX.X<CR><LF>

where X.X is the current software version level (for example, 1.0).

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SYSFAIL, Self Test, And Initialization

The VX4240 Module will execute a self test at power-up, or upon direction of a VXIbus hard or soft reset condition, or upon command. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4240's commander, sets the Reset bit in the VX4240's Control register.

During a power-up, or hard or soft reset, the following actions take place:

1) The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing a self test, and the Failed LED is lit. If this is a commanded self test, SYSFAIL* is not asserted. In the case of a soft reset, SYSFAIL* is set. However, all Tek/CDS commanders, such as the VX4520 ##, will simultaneously set SYSFAIL INHIBIT. This is done to prevent the resource manager from prematurely reporting the failure of a module.

2) Once the self test is complete, the SYSFAIL* line is released, and the module enters the VXIbus PASSED state (ready for normal operation). SYSFAIL* will be released within five seconds in normal operation.

   If the self test fails, the module makes an internal record of what failure(s) occurred, which allows an error message to be returned to the module's commander.

The default condition of the VX4240 Module after the completion of power-up self test is as follows:

Mode: software trigger
Collect: Post-trigger, count = RAMsize - 100
Level 1: +100
Level 2: -100
Voltage: ±100V, dc coupled, 1 MOhm input impedance, single-ended input.
Frequency: 10 MHz, internal clock
Delay: 0
All interrupts disabled
All control I/O signals negative edge triggered
VXI output trigger disabled
Real time update frequency: 10 MHz
Block delimiter: semi-colon

Self test can also be run at any time during normal operation by using the S command. At the end of a self test initiated by the S command, the module is restored to its power-up state.

During a commanded self test:

1) SYSFAIL* is not asserted.

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2) The module executes an extended self test.

3) The module always returns to its default state after self test.

SYSFAIL* Operation

SYSFAIL* becomes active during power-on, hard or soft reset, self test, or if the module loses any of its power voltages. When the mainframe Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4240 Module to deactivate SYSFAIL* in all cases except when power is lost.

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Section 4
Programming Examples

This section contains example programs which demonstrate how the various programmable features of the VX4240 are used. The examples are written in BASIC using an IBM PC or equivalent computer as the system controller.

Definition of BASIC Commands

The programming examples in this manual are written in Microsoft GW BASIC. These examples use the GW BASIC commands described below. If the programming language you are using does not conform exactly to these definitions, use the command in that language that will give the same result.

Command — Result

CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)
The CALL ENTER statement inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the input, the variable LENGTH% contains the number of bytes read from the instrument. The variable STATUS% contains the number '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. Prior to using the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the VX4240.

CALL SEND (ADDRESS%, WRT$, STATUS%)
The CALL SEND statement outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the output of data, the variable STATUS% contains a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.

END Terminates the program.

FOR/NEXT
Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.

GOSUB n
Runs the subroutine beginning with line n. EX: GOSUB 750 - runs the subroutine beginning on line 750. The end of the subroutine is delineated with a RETURN statement. When the subroutine reaches the RETURN statement, execution will resume on the line following the GOSUB command.

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GOTO n

Program branches to line n. EX: GOTO 320 - directs execution to continue at line 320.

IF/THEN

Sets up a conditional (IF/THEN) statement. Used with other commands, such as PRINT or GOTO, so that IF the stated condition is met, THEN the command following is effective. EX: IF I = 3 THEN GOTO 450 - will continue operation at line 450 when the value of variable I is 3.

REM or '

All characters following the REM command or a ' are not executed. These are used for documentation and user instructions. EX: REM **CLOSE ISOLATION RELAYS**

RETURN

Ends a subroutine and returns operation to the line after the last executed GOSUB command.

<CR>

Carriage Return character, decimal 13.

<LF>

Line Feed character, decimal 10.

Programming Example In BASIC

The following sample BASIC program shows how commands for the VX4240 might be used. This example assumes that the VX4240 has logical address 24 and is installed in a VXIbus mainframe that is controlled via an IEEE-488 interface from an external system controller, such as an IBM PC or equivalent using a Capital Equipment Corp. IEEE-488 interface. The VXIbus IEEE-488 interface is assumed to have an IEEE-488 primary address of decimal 21 and to have converted the VX4240 module's logical address to an IEEE-488 primary address of decimal 24. Lines which are indented and not numbered are comments which clarify what the program is doing at those points.

Lines 10 through 70 initialize the PC's IEEE-488 interface module.

```
10 DEF SEG = &HC400
```

Defines memory location for PCX I/O card.

```
15 GOSUB 1000
```

Determine memory location of CEC card.

```
20 INIT = 0
```

Initialize PROM offsets for PCX I/O card.

```
30 SEND = 9: ENTER = 21
40 PC.ADDRESS% = 0
```

Defines I/O card address.

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```
50 ADDR4240% = 24
```
Defines VX4240's IEEE-488 address.
```
60 CONTROL% = 0
```
Defines I/O card as a bus controller.
```
70 CALL INIT(PC.ADDRESS%,CONTROL%)
80 RD$ = SPACE$(8)
```
Allocate space for the input string variable.
```
90 TM$ = CHR$(10)
```
Define Line Feed terminator.
```
100 CLS
```
Clear the screen.
```
110 WRT$ = "R" + TM$
```
Send the card a RESET command.
```
120 CALL SEND(ADDR4240%,WRT$,STATUS%)
```
Output the reset message.
```
130 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
```
Read the default response. The card should respond with "S00000". Note that the status response (see the "Q" command) is the only response from the card that begins with an "S".
```
140 PRINT "DEFAULT MESSAGE -> " + RD$
150 RD$ = SPACE$(200)
160 WRT$ = "EA" + TM$
```
Issue an ERROR (E) command to the card, and read the result back. The card should respond with "NO ERRORS".
```
170 CALL SEND(ADDR4240%,WRT$,STATUS%)
180 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
190 PRINT "ERROR RESPONSE -> " + RD$
200 WRT$ = "F1E6;V5;T" + TM$
```
Set the card to sample at 1 Mhz on the ±5 volt range and trigger the card. Note that the ";" following "F1E6" AND "V5" delimit each of the commands, while TM$ delimits the trigger command and the command string.
```
210 CALL SEND(ADDR4240%,WRT$,STATUS%)
220 RD$ = SPACE$(8)
230 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
```
Read back the status response. While the card is sampling, the response will be "S00110". When the memory is filled, the response is "S00011". Loop here until the memory is full.
```
240 IF MID$(RD$,6,1) = "0" GOTO 230
250 PRINT "MEMORY FULL, STATUS RESPONSE -> " + RD$
```
Now that the memory is full, the A commands can be used to look at the data. Issue the AX command to read the maximum value in memory.
```
260 WRT$ = "AX" + TM$
270 CALL SEND(ADDR4240%,WRT$,STATUS%)
280 RD$ = SPACE$(31)
290 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
300 PRINT "MAXIMUM VALUE ->" + RD$
```
Example data returned from the above sequence is XV = +2.9248047E+000 (0021263) indicating a maximum value 2.9248047 volts at address 21263. To look at the data at this location, the INPUT (I) command is used with the offset determined by reading in the location value from the AX response.
```
310 OFFSET$ = MID$(RD$,22,7)
```


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```
320 WRT$ = "I" + OFFSET$ + TM$
330 CALL SEND(ADDR4240%,WRT$,STATUS%)
340 RD$ = SPACE$(14)
350 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
      Example data returned is +002.9248046
360 PRINT "DATA VALUE LOCATION " + OFFSET$ + " -> " + RD$
      To look at the data at the next location (address 21264), issue another read.
370 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
380 PRINT "NEXT DATA VALUE -> " + RD$
      Find the maximum positive transition in memory.
390 WRT$ = "AP" + TM$
400 CALL SEND(ADDR4240%,WRT$,STATUS%)
410 RD$ = SPACE$(31)
420 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
430 PRINT "MAXIMUM POSITIVE TRANSITION -> " + RD$
      Example data returned is PT= +2.2216797E-001 (0002307). To look at four data values
      beginning at the maximum transition, the INPUT BLOCK command can be used, again getting
      the address from the response.
440 OFFSET$ = MID$(RD$,22,7)
450 WRT$ = "I" + OFFSET$ + "K4" + TM$
460 CALL SEND(ADDR4240%,WRT$,STATUS%)
470 RD$ = SPACE$(4 * 13 + 2)
480 CALL ENTER(RD$,LENGTH%,ADDR4240%,STATUS%)
      Example data returned is +000.1708984;+000.3930664;+000.5371093;+000.7177734;
490 PRINT "POSITIVE TRANSITION DATA"
500 PRINT RD$
510 INPUT "TYPE ENTER TO END PROGRAM",DUMMY$
520 END

1000 '  SUB ROUTINE IDENTIFIES THE MEMORY LOCATION OF
1010 '  CEC IEEE-488 INTERFACE CARD ROM
1020 '
1030 FOR I = &H40 TO &HEC STEP &H4
1040 FAILED =0: DEF SEG = (I * &H100)
1050 IF CHR$ ( PEEK (50) ) < > "C" THEN FAILED =1
1060 IF CHR$ ( PEEK (51) ) < > "E" THEN FAILED =1
1070 IF CHR$ ( PEEK (52) ) < > "C" THEN FAILED =1
1080 IF FAILED = 0 THEN CECLOC = (I * &H100 ): I = &HEC
1090 NEXT I
1100 RETURN
```


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Appendix A
VXIbus Operation

The VX4240 Module is a C size single slot VXIbus Message Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The VX4240 Module is neither a VXIbus commander nor a VMEbus master, and therefore it does not have a VXIbus signal register. The VX4240 is a VXIbus message based servant.

The module supports both the Normal Transfer Mode and the Fast Handshake Mode of the VXIbus, using the Write Ready, Read Ready, DOR and DIR bits of the module's Response register.

A Normal Transfer Mode Read of the VX4240 Module proceeds as follows:

1. The commander reads the VX4240's Response register and checks if the Write Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll the bits until they become true.

2. The commander writes the Byte Request command (0DEFFh) to the VX4240's Data Low register.

3. The commander reads the VX4240's Response register and checks if the Read Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Read Ready bit until it becomes true.

4. The commander reads the VX4240's Data Low register.

A Normal Transfer Mode Write to the VX4240 Module proceeds as follows:

1. The commander reads the VX4240's Response register and checks if the Write Ready and DIR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll the bits until they become true.

2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX depending on the state of the End bit) to the VX4240's Data Low register.

The VX4240 Module also supports the Fast Handshake mode during some commands. In this mode, the module is guaranteed to return DTACK* within the 20 microsecond window defined by the VXIbus Specification. The VX4240 Module asserts BERR* to

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switch from Fast Handshake Mode to Normal Transfer Mode. The VX4240's Read Ready and Write Ready bits react properly during Fast Handshake.

A Fast Handshake Transfer Mode Read of the VX4240 Module proceeds as follows:

1. The commander writes the Byte Request command (0DEFFh) to the VX4240's Data Low register.

2. The commander reads the VX4240's Data Low register.

A Fast Handshake Transfer Mode Write to the VX4240 Module proceeds as follows:

The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX depending on the state of the End bit) to the VX4240's Data Low register.

The VX4240 Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the Data Low register, the Response register or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the VX4240's address space will have no affect on the operation of the module.

CAUTION

If the card cage has other manufacturer's computer boards operating in the role of VXIbus foreign devices, the assertion of BERR (as defined by the VXIbus Specification) may cause operating problems on these boards.*

As with all VXIbus devices, the VX4240 module has registers located within a 64 byte block in the A16 address space.

The base address of the VX4240 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set by the Logical Address switches, or, in dynamic configuration, as set by the module's commander.

VX4240 Configuration Registers

Below is a list of the VX4240 Configuration Registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The offset is relative to the module's base address.

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REGISTER DEFINITIONS

Register	Address	Type	Value (Bits 15-0)
ID	0000H	RO	1011 1111 1111 1101 (BFFCh)
Logical Address	0000H	WO	See Logical Address definition below
Device Type	0002H	RO	See Device Type definition below
Status	0004H	RO	See Status definition below
Control	0004H	WO	See Control definition below
Offset	0006H	RO	1111 1111 1111 1111 (FFFFh)
Protocol	0008H	RO	1111 0111 1111 1111 (F7FFh)
Response	000AH	RO	Defined by state of the interface
Data High	000CH		Not used
Data Low	000EH	W	See Data Low definition below

BIT DEFINITIONS

Register	Bit Location	Bit Usage	VX4240 Value	VX4240 Usage
ID	15-14	Device Class	10	Message Based
	13-12	Address Space	11	A16 only
	11-0	Manufact. ID	1111 1111 1101	Tektronix
Logical Addr.	15-8	Logical Address	xxxx xxxx	Not used
	7-2		xxxx xxxx	Defines the logical address during dynamic configuration. Once a value other than FFH is written to this register, all other writes will have no effect.
Device Type	15-0	Device Type	1111 1101 1111 0111	
Status	15	A24/32 Active 1		Not used
	14	MODID*	1	MODID line not active
			0	MODID line active
	13-4	Device dependent	11 1111 1111	Not used
	3	Extended*	1	Not used
	2	Passed	1	Passed self test.
			0	Failed self test.
	1-0	Device dependent	11	Not used

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BIT DEFINITIONS (continued)

Register	Bit Location	Bit Usage	VX4240 Value	VX4240 Usage
Control	15	A24/32 Enable	1 or 0	No effect
	14-2	xxxx xxxx	111 1111 1111 11	xxxx xx
	1	SYSFAIL Inhibit	1	Disables module from driving Sysfail
			0	Enables module to drive Sysfail
	0	Reset	1	Reset
			0	Not reset
Offset	15-0	Offset	1111 1111 1111 1111	Indicates there is only one device using the address decoding hardware.
Protocol	15	CMDR*	1	Servant only
	14	Signal Reg.*	1	No Signal Reg.
	13	Master*	1	Slave only
	12	Interrupter	1	Interrupter
	11	FHS*	0	Fast Handshake capability
	10	Shared Memory*	1	No Shared Memory capability
	15	Defined value of 0	0	Per VXI
	9-4	Reserved	11 1111	Not used
	3-0	Device dependent	1111	Not used
Response	14	Reserved	1	Per VXI
	13	DOR	1	Module is ready to return data via Byte Request command.
			0	Module is not ready to return data via Byte Request command.
	12	DIR	1	Module is ready to accept data via Byte Available command.
			0	Module is not ready to accept data via Byte Available command.
	11	ERR*	1	No Word Serial Protocol errors detected.
			0	Word Serial Protocol error detected.

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BIT DEFINITIONS (continued)

Register	Bit Location	Bit Usage	VX4240 Value	VX4240 Usage
	10	Read Ready	1 or 0	Indicates that the instrument portion of the module has data available to be read. Set by the instrument following a "Byte Request" command, and cleared on a read from the Data Low register or on reset.
	9	Write Ready	1 or 0	Cleared upon receipt of any Word Serial command. Set when the instrument is ready to receive another Word Serial command.
	8	FHS Active*	0	FHS active
			1	FHS inactive
	7	Locked*	1	Not used
	6-0	Device dependent	111 1111	Not used

Data High - not implemented.

Data Low (read/write)

Word Serial Commands

A write to the Data Low register causes this module to execute some action based on the data written. This section describes the device specific Word Serial commands this module responds to and the results of these commands.

Abort Normal Operation Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1

When this command is received, the module responds as follows:

- Any pending VXIbus interrupts are cleared.
- Generation of the Request True event is enabled (see Control Event command).
- The DIR bit in the Response register is set to 1 (active).
- The ERR* bit in the Response register is set to 1 (inactive state).
- The FHS* bit in the Response register is set to 1 (inactive state).
- Generation of VXIbus interrupts is disabled (requires a Begin Normal Operation command to be re-enabled).
- The Read Ready bit in the Response register is set to 1 (active).
- The Write Ready bit in the Response register is set to 1 (active).

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- Any module-specific configuration information will return to its power-up default state.

A read of the Data Low register following this command will return the following data:

Response Data:
Bits 15-0 1111 1111 1111 1110

Asynchronous Mode Control Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	1	0	0	0	x	x	x	x	x	Event En*	x	Event Mode

Event En*: 1 Disables generation of events
0 Enables generation of events

Event Mode*: 0 Any value other than 0 will disable event operation. Events will always be sent as interrupts.

When this command is received, the enabling/disabling of event interrupts will occur immediately. A read of the Data Low register following this command will return the following data:

Not used: Bits 15-13 1111 1111 1111 1110

Event En*: Bit 2 1 if event generation has been disabled.
0 if event generation has been enabled.

Not used: Bit 1 1

Event Mode: Bit 0 0

Begin Normal Operations Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	0	x	1	1	1	1	1	1	1	1

This command enables the generation of Request True interrupts of the VXIbus backplane. For interrupts to be generated, this command and the module-specific command must both be received.

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Byte Available Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	1	0	x	x	x	x	x	x	x	x	x

This command is used to transfer module-specific commands and data to the module.

Byte Request Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	1	1	0	1	1	1	1	1	1	1	1

This command is used to request module-specific data. A read of the Data Low register following this command will return the following data:

Not used:

Bits 15-9 1111 111

End:

Bit 8	1	Indicates the module is returning an ASCII line feed character ad data. Normally indicates the end of a module-specific data return sequence.
	0	Binary data or non-line feed ASCII characters are being returned as data.

Datum:

Bits 7-0		
	xxxx xxxx	Actual data item being returned.

Clear Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

When this command is received, the module responds as follows:

- The Read Ready bit in the Response register is set to 0 (inactive).
- The ERR* bit in the Response register is set to 1 (inactive).

Control Event Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	1	1	1	1	ENB	Event						

This command controls the enabling/disabling of the Request True event.

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Enb:	0	Disables the event described in the lower 7 bits.
	1	Enables the event described in the lower 7 bits.
Event:	111 1101	Request True event value. Any other value for Event will have no effect.

End Normal Operation Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1

When this command is received, the module responds as follows:

- Any pending VXIbus interrupts are cleared.
- The DIR bit in the Response register is set to 1 (active).
- The ERR* bit in the Response register is set to 1 (inactive state).
- The FHS* bit in the Response register is set to 1 (inactive state).
- Generation of VXIbus interrupts is disabled (requires a Begin Normal Operation command to be re-enabled).
- The Read Ready bit in the Response register is set to 1 (active).
- The Write Ready bit in the Response register is set to 1 (active).
- If enabled, the module receivers will be disabled.

A read of the Data Low register following this command will return the following data:

Response Data:
Bits 15-0 1111 1111 1111 1110

Error Query Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1

This command will cause the module to place the first unreported Word Serial Protocol encountered into the Data Low register.

A read of the Data Low register following this command will return the following data:

No errors encountered:
Bits 15-0 1111 1111 1111 1111

Multiple Word Serial queries:
Bits 15-0 1111 1111 1111 1101

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Unrecognized command:
Bits 15-0 1111 1111 1111 1100

In addition, when the Data Low register is read, the ERR* bit in the Response register will be set to 1 (inactive).

Read Protocol Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

If the Data Low register is read after this command, the contents are as follows:

VXIbus Version Level:
Bit 15
1 VXIbus Version 1.4 Device

Device dependent (unused):
Bits 14 13 12 11
1 1 1 1

Reserved:
Bits 10 9 8
1 1 1

E*:
Bit 7
0 This module does support the Error Query command.

PI*:
Bit 6
0 IF the Interrupt switch is set to 0,
ELSE
1 This module does not support Read Interrupters, Read Interrupter Line, and Assign Interrupter Line commands.

PH*:
Bit 5
1 This module does not support the Read Handlers, Read Handler Line, and Assign Handler Line commands.

Triggered*: (supports trigger command)
Bit 4
0 This module supports the trigger command.

I4*: (supports VXIbus 488.2 Instrument protocol)
Bit 3
1 This module does not support 488.2 protocol.

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I*: (supports VXIbus instrument protocol)
Bit 2
0 This module supports instrument protocol.

ELW*: (supports Extended Longword Serial protocol)
Bit 1
1 This module does not support ELW protocol.

LW*: (supports Longword Serial protocol)
Bit 0
1 This module does not support LW protocol.

Read STB Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1

This command is used to place a status word in the Data Low register. A read of the Data Low register following this command will return data in the following format:

Not used: Bits 15-7 1111 1111 0

Service Request:
Bit 6
1 If the module has asserted an interrupt line and has been acknowledged.
0 If the module has not asserted an interrupt line or if an asserted interrupt has not been acknowledged.

Not used: Bits 5, 4 11

Channel 4:
Bit 3 1, 0 The channel 4 bit is 1 if the interrupt was caused by the module's channel 4.

Channel 3:
Bit 2 1, 0 The channel 3 bit is 1 if the interrupt was caused by the module's channel 3.

Channel 2:
Bit 1 1, 0 The channel 2 bit is 1 if the interrupt was caused by the module's channel 2.

Channel 1:
Bit 0 1, 0 The channel 1 bit is 1 if the interrupt was caused by the module's channel 1.

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VX4240 Interrupts

The VX4240 will interrupt its commander with a Request True event when all the following conditions have been met:

- The interrupt level is set to level 1-7.
- The module has received a Begin Normal Operation command.
- Generation of the Request True event is enabled. (This is the power-up default state, equivalent to receiving a Control Event command enabling the Request True event.)
- Generation of events has been enabled. (This is the power-up default state, equivalent to receiving the Asynchronous Mode Control command enabling event interrupts.)
- Reception of the module-specific command IN (see B command), enabling interrupts.

The module will respond with the following data when the IACK cycle for the interrupt level chosen occurs:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 1  1  1  1  1  1  0  1  <--Logical Address--->
```

A new interrupt can only be generated after the previous interrupt has been acknowledged and the Word Serial Read STB command has been received by the module.

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Appendix B
Input/Output Connections

Analog Input [SIG + (J1); SIG- (J2)]
These connectors provide the signal interface to the VX4240 Module. SIG + corresponds to the high side of a differential signal, and SIG- for the low side. Single-ended signals should use only SIG + as the signal input.

Gate Input (S3-7)
The Gate input is used to inhibit sampling of the VX4240 Module. If active, the Gate input inhibits data collection, the threshold triggers, the real time update counters, and the delay (sample) counters. The Gate input does not affect the arm signals or any of the other triggers. Used in conjunction with the various trigger modes of the VX4240 Module and the external clock input, very precise control of the sampled data can be achieved. The Gate input is an active low TTL signal.

External Clock Input (S3-13)
The external clock input allows control of the sampling rate of the VX4240 Module. The clock can be varied up to a maximum frequency of 10MHz. Any duty cycle is permitted, with the constraint that the minimum clock-high and clock-low times are 50 ns each. Data is sampled on the low-to-high transition of the clock. The external clock is a TTL level input terminated in 50 Ohms.

External Trigger Input (S3-11)
The external trigger input allows control of when the VX4240 Module begins sampling data. This is a TTL level edge-triggered signal, with the active edge programmable to either high or low.

Trigger Out (S3-10)
The trigger out signal is a TTL output indicating that the VX4240 Module trigger event has occurred, programmable to either active high or active low true. Once the trigger has occurred, this signal remains active until the trigger is rearmed, or the module is reset.

Clock Out (S3-12)
The clock out signal corresponds to the frequency of the sampling clock. Clock out is a 50% duty cycle, TTL level signal, and is active only while the VX4240 Module is sampling data. Clock out uses a 50 Ohm line driver circuit.

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ARM IN (S3-9)
The arm in input allows you to control when the triggers are armed. It is an edge triggered input, programmable to either positive or negative edge true.

ARMED (S3-8)
The armed output is a TTL output indicating that the triggers have been armed. It is programmable to either positive or negative edge triggered true.

SIG IN+ (S3-1); SIG IN- (S3-2)
These inputs are the same as SIG+ and SIG-but brought in through the DB25 connector to make cabling easier. These inputs are enabled (SIG+/SIG- disabled, and vice versa) under program control.

ANALOG (SIGNAL) GROUND
S3-3, S3-14, S3-15, S3-16, J1 Shield (outer conductor), J2 Shield.

DIGITAL GROUND
S3-6, S3-19, S3-20, S3-21, S3-22, S3-23, S3-24, S3-25.

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Appendix C
VXIbus Glossary

The terms in this glossary are defined as used in the VXIbus System. Although some of these terms may have different meanings in other systems, it is important to use these definitions in VXIbus applications. Terms which apply only to a particular instrument module are noted. Not all terms appear in every manual.

Term	Definition
Accessed Indicator	An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.
ACFAIL*	A VMEbus backplane line that is asserted under these conditions: 1) by the card cage Power Supply when a power failure has occurred (either ac line source or power supply malfunction), or 2) by the front panel ON/STANDBY switch when switched to STANDBY.
A-Size Card	A VXIbus instrument module that is 100.0 by 160 mm by 20.32 mm (3.9 by 6.3 in by 0.8 in), the same size as a VMEbus single-height short module.
Asynchronous Communication	Communications that occur outside the normal "command-response" cycle. Such communications have higher priority than synchronous communication.
Backplane	The printed circuit board that is mounted in a VXIbus card cage to provide the interface between VXIbus modules and between those modules and the external system.
B-Size Card	A VXIbus instrument module that is 233.4 by 160 mm by 20.32 mm (9.2 by 6.3 in by 0.8 in), the same size as a VMEbus double-height short module.
Bus Arbitration	In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.
Bus Timer	A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-

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existent Slave location could result in an infinitely long wait for the Slave response.

Client — In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10 — A 10-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P2. It is distributed to each module slot as a single source, single destination signal with a matched delay of under 8 ns.

CLK100 — A 100-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P3. It is distributed to each module slot in synchronous with CLK10 as a single source, single destination signal with a maximum system timing skew of 2 ns, and a maximum total delay of 8 ns.

Commander — In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

Command — A directive to a device. There are three types of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

Communication Registers — In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

Configuration Registers — A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

C-Size Card — A VXIbus instrument module that is 340.0 by 233.4 mm by 30.48 mm (13.4 by 9.2 in by 1.2 in).

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Custom Device A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

Data Transfer Bus One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

DC SUPPLIES Indicator A red LED indicator that illuminates when a DC power fault is detected on the backplane.

Device Specific Protocol A protocol for communication with a device that is not defined in the VXIbus specification.

D-Size Card A VXIbus instrument module that is 340.0 by 366.7 mm by 30.48 mm (13.4 x 14.4 in x 1.2 in).

DTB See Data Transfer Bus.

DTB Arbiter A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

DUT Device Under Test.

ECLTRG Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 ohms; the asserted state is logical High.

Embedded Address An address in a communications protocol in which the destination of the message is included in the message.

ESTST Extended STart/STop protocol; used to synchronize VXIbus modules.

Extended Self Test Any self test or diagnostic power-up routine that executes after the initial kernel self test program.

External System Controller The host computer or other external controller that exerts overall control over VXIbus operations.

FAILED Indicator A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

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IACK Daisy Chain Driver The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

ID-ROM An NVRAM storage area that provides for non-volatile storage of diagnostic data.

Instrument Module A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus card cage. An instrument module may contain more than one device. Also, one device may require more than one instrument module.

Interface Device A VXIbus device that provides one or more interfaces to external equipment.

Interrupt Handler A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

Interrupter A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

IRQ The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

Local Bus A daisy-chained bus that connects adjacent VXIbus slots.

Local Controller The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus card cage or several card cages. See Resource Manager.

Local Processor The processor on an instrument module.

Logical Address The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.

Mainframe **Card Cage** For example, the Tektronix VX1400 Card Cage, an operable housing that includes 13 C-size VXIbus instrument module slots.

Memory Device A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

Message A series of data bytes that are treated as a single communication, with a well defined terminator and message body.

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Message Based Device — A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

MODID Lines — Module/system identity lines.

Physical Address — The address assigned to a backplane slot during an access.

Power Monitor — A device that monitors backplane power and reports fault conditions.

P1 — The top-most backplane connector for a given module slot in a vertical card cage such as the Tektronix VX1400. The left-most backplane connector for a given slot in a horizontal card cage.

P2 — The bottom backplane connector for a given module slot in a vertical C-size card cage such as the VX1400; or the middle backplane connector for a given module slot in a vertical D-size card cage such as the VX1500.

P3 — The bottom backplane connector for a given module slot in a vertical D-size card cage such as the Tektronix VX1500.

Query — A form of command that allows for inquiry to obtain status or data.

READY Indicator — A green LED indicator that lights when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5-volt power will extinguish this indicator.

Register Based Device — A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.

Requester — A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.

Resource Manager — A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self test diagnostics, and initializing system commanders.

Self Calibration — A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.

Self Test — A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self test routine is performed upon power-up.

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Servant	A VXIbus message-based device that is controlled by a commander.
Server	A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.
Shared Memory Protocol	A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.
Slot 0 Controller	See Slot 0 Module. Also see Resource Manager.
Slot 0 Module	A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.
SMP	See Shared Memory Protocol.
STARX	Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a card cage. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.
STARY	Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a card cage. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.
STST	STart/STop protocol; used to synchronize modules.
SYNC100	A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100. These signals are individually buffered and matched to less than 2ns of skew.
Synchronous Communications	A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.
SYSFAIL*	A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.
System Clock Driver	A functional module that provides a 16-MHz timing signal on the Utility Bus.

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System Hierarchy The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

Test Monitor An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.

Test Program A program, executed on the system controller, that controls the execution of tests within the test system.

Test System A collection of hardware and software modules that operate in concert to test a target DUT.

TTLTRG Open collector TTL lines used for inter-module timing and communication.

VXIbus Subsystem One card cage with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.

Word Serial Protocol A VXIbus word oriented, bi-directional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).

Word Serial Communications Inter-device communications using the Word Serial Protocol.

WSP See Word Serial Protocol.

10-MHz Clock A 10 MHz, ±100 ppm timing reference. Also see CLK10.

100-MHz Clock A 100 MHz, ±100 ppm clock synchronized with CLK10. Also see CLK100.

488-To-VXIbus Interface A message based device that provides for communication between the IEEE-488 bus and VXIbus instrument modules.

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Appendix D
Triggering Collection Control

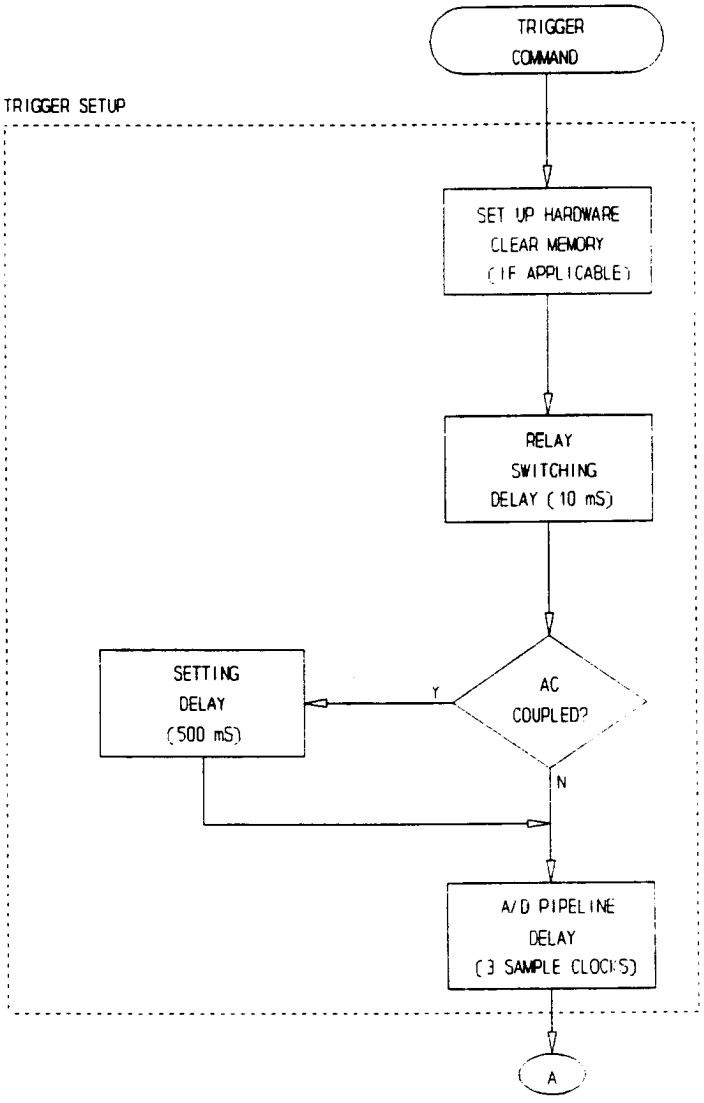

Figure 7: Trigger Setup

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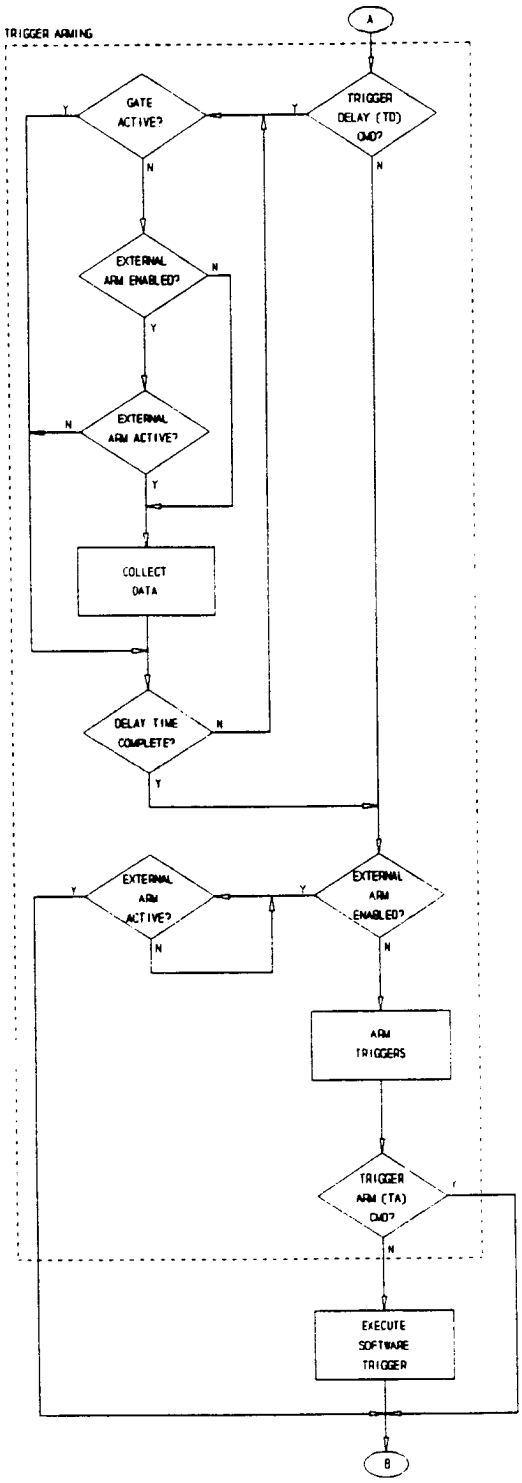

Figure 8: Trigger Arming

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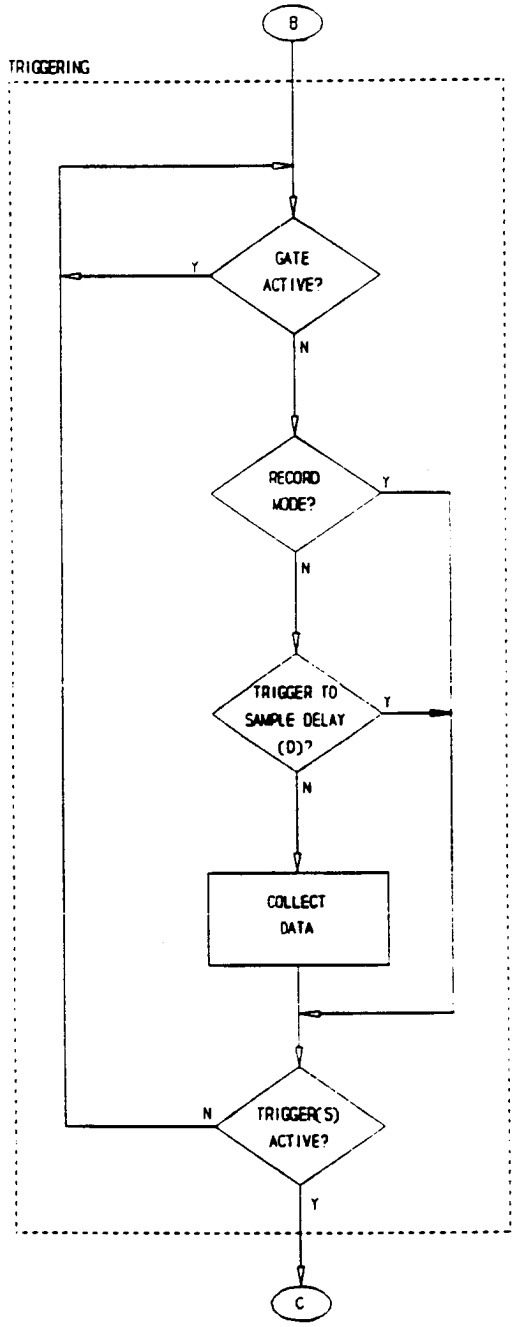

Figure 9: Triggering

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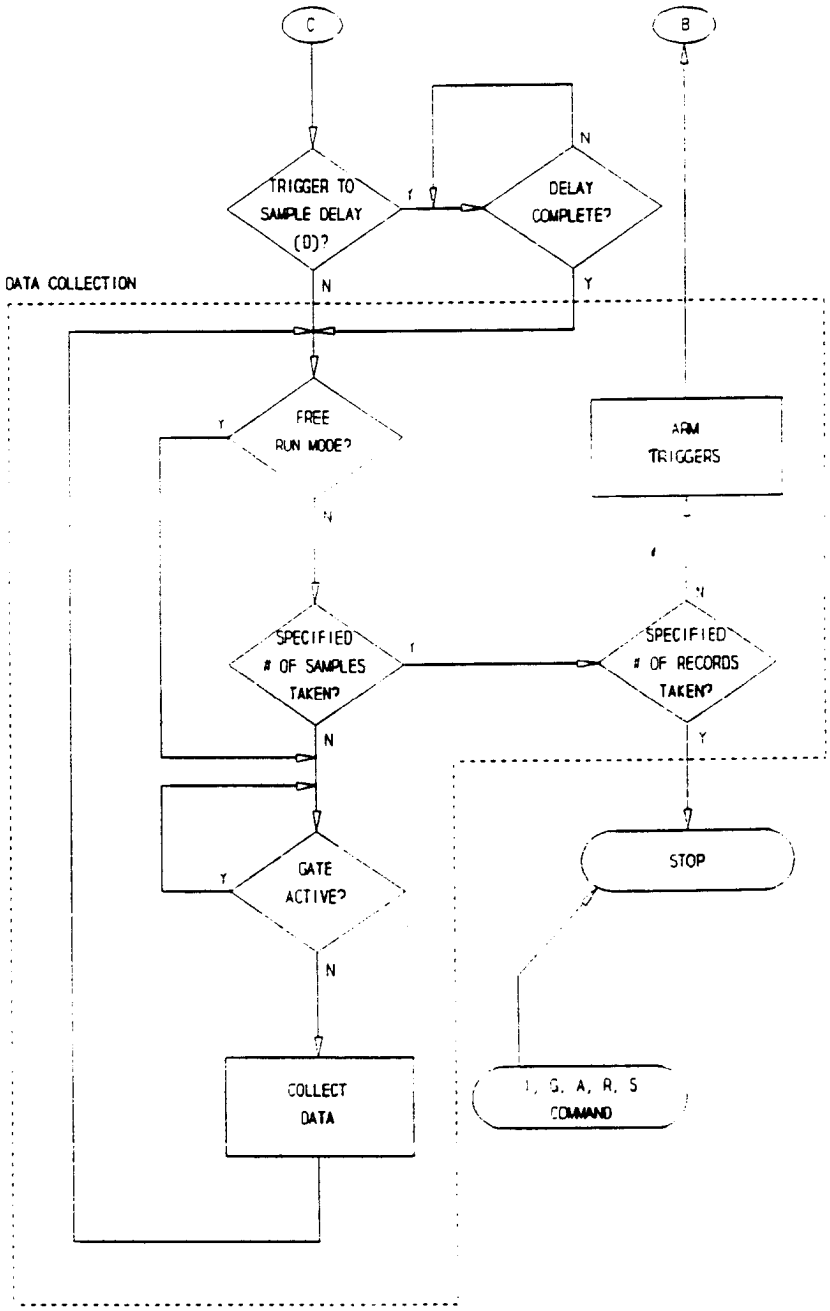

Figure 10: Data Collection

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Appendix E
Using The Fourier Transform For Sampled Signals

The following is a brief discussion of the basic principles of Fourier transform theory. For more information on the subject refer to The Fast Fourier Transform by E. Oran Brigham, published in 1974 by Prentice-Hall, Incorporated.

The Fourier transform is a method for converting a time domain sample signal into the frequency domain to provide a spectral representation of the sample signal. The spectral representation is obtained by decomposing a waveform into a sum of sinusoids of different frequencies. The Fourier transform identifies the different frequency sinusoids (and their respective amplitudes) which combine to produce a waveform.

The discrete Fourier transform approximates the continuous Fourier transform for sampled signals. The fast Fourier transform (FFT) is a method of performing a series of computations to compute the discrete Fourier transform more quickly.

The discrete Fourier transform approximates the continuous transform when the sampling interval T is sufficiently small. If T is chosen too large, distortion of the Fourier transform occurs. This distortion, known as 'aliasing', introduces invalid frequency components into the transform. Aliasing occurs because the time function was not sampled at a sufficiently high rate to accurately represent the signal. To minimize aliasing, the sampling frequency F must be chosen to be a minimum of twice the frequency of the highest frequency component f(c) of the signal. This may be written

$$F = 1/T = 2f(c)$$

where sampling frequency F is known as the Nyquist sampling rate, and the Fourier transform is said to be band-limited at the highest frequency f(c). In other words, the Fourier transform is ideally zero for frequencies above f(c). It should be noted that rarely can a waveform be band- limited. To minimize aliasing effects, the signal should be sampled at a rate such that aliasing becomes negligible, and low pass filtered, to the extent possible, to approach band-limiting.

Since the discrete transform is considered over infinity, it is necessary to truncate the sampled signal for digital analysis, because only a finite number of samples (N) can be taken. The effect of this truncation is to convolve a sin(x)/x factor into the transform, which causes leakage into the frequency components of the adjacent cells. By increasing N (the number of points in the transform), the sin(x)/x factor more closely approximates an impulse, and less error is introduced.

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Also note that since the Fourier transform is periodic, the discrete transform also requires periodicity. In order to best approximate the continuous transform, an integral number of cycles of the time domain waveform needs to be contained within the sample period. If the truncation interval is a multiple of the period, the frequency domain sampling function will coincide with the zeros of the sin(x)/x function, canceling its effect. This is called coherency.

To summarize, the class of waveforms for which the discrete and continuous Fourier transforms are approximately the same requires that:

1) the sampling rate be at least twice the frequency of the highest frequency component of the time function;

2) the time function be band-limited (no frequencies must exist above one-half the sampling frequency);

3) the time function be periodic; and

4) an integer multiple of the cycles of the time function be within the sample period.

If the signal is band-limited and periodic, but the truncation interval is not equal to an integer multiple of the time period (non-coherent), the following errors result:

- The frequency function has an impulse at zero frequency representing the average value of the truncated waveform. This occurs because the signal does not average out to zero over time, and causes a dc component to appear in the spectrum.

- The frequency function no longer appears as a single impulse, but rather as a continuous function of frequency, with a local maximum centered at the original frequency, and a series of other peaks termed side-lobes. These side-lobes are introduced by the sin(x)/x factor, and are responsible for the additional frequency components which occur in the spectral representation. This effect is called 'leakage', and is inherent in the discrete transform because of time domain truncation.

To reduce this leakage, it is necessary to employ a time domain truncation function which has side-lobe characteristics of smaller magnitude than those of the sin(x)/x function. The smaller the side-lobes, the less leakage in the discrete transform.

The Hanning function (AH command) is a particularly good truncation (windowing) function, and is given by

$$x(t) = \frac{1}{2} - \frac{1}{2} [\cos (2\pi t) / Tc]$$

where t is the relative time of the sample, and Tc is the truncation interval. This significantly reduces the leakage. However, reducing the leakage means that the non-zero frequency components are considerably broadened or smeared with respect to the impulse function.

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Another good truncation function is the Blackman-Harris window (AQ command). This further narrows the leakage around the fundamental frequency.

If the input signal is an integer multiple of the FFT frequency resolution, no truncation factors are required (or desired). Since real world signals are generally complex, or pulse-like, and rarely occur at a multiple of the frequency resolution, it is generally good practice to use the windowing functions to obtain more accurate representation of the frequency domain.

The frequency resolution of an FFT is

(sampling frequency)/(FFT size)

For example, if the sampling frequency is 10 MHz, and a 1024 point FFT is performed, the resolution of each frequency component (512 total) is 10e6/1024, or 9.76563 KHz. Since the first component is is DC (0 Hz), the total represented spectrum is 511 * 9.76563 KHz, or 4.99023 MHz.

Note that increasing the FFT size increases the frequency resolution. For example, a 2048 point FFT resolves each slice to 4.88281 KHz. The cost, though, is that a 2048 point FFT takes approximately twice as much time as a 1024 point FFT.

The total harmonic distortion (THD) is the relationship between the amplitude of the fundamental frequency (f_s) relative to the first five harmonics, which are at $2*f_s$, $3*f_s$, $4*f_s$, $5*f_s$, and $6*f_s$. For example, if the fundamental is at 1.40625 MHz, the second harmonic is at 2.8125 MHz, the third at 4.21875 MHz, etc.

Using this example, note that the fourth through sixth harmonics are beyond the frequency spectrum (Nyquist) of the FFT (5 MHz for a sampling frequency of 10 MHz). Because they are greater than the Nyquist frequency, they are aliased, or folded back onto frequency components below the Nyquist rate. The fourth harmonic (5.625 MHz) would be aliased back to 4.375 MHz, the fifth (7.03125 MHz) to 2.98765 MHz, and the sixth (8.4375 MHz) to 1.5625 MHz. These higher frequencies are effectively a mirror image of the 5 MHz spectrum. The D option of the FFT command returns the amplitudes and frequencies of the fundamental and the harmonics.

Because of this aliasing effect, care must be taken in selecting the fundamental frequency to ensure that a harmonic is not aliased onto the fundamental frequency, causing an invalid THD measurement. To prevent this, the fundamental frequency cell (or bin) should be a prime number (1, 3, 5, 7, 11, 17, etc.):

$$\frac{\text{input frequency}}{\text{sampling frequency}} = \frac{N \text{ (prime number)}}{M \text{ (size of FFT)}}$$

Signal-to-noise ratio (SNR) is the relationship of the amplitude of the fundamental frequency to the amplitude of all the other frequencies, excluding the five harmonic frequencies. Signal-to-noise and distortion (SINAD) is the relationship of the fundamental amplitude to all other frequencies including the harmonics. Spurious free

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dynamic range (SFDR) is the difference between the amplitude of the fundamental and the amplitude of the next highest harmonic or noise spur.

The amplitude of the fundamental frequency is the reference for THD, SNR, SINAD, and SFDR measurements, and is referred to as the carrier frequency. So these measurements are all in dBc (decibels below the carrier).

To improve the accuracy of these measurements, a three cell summation is employed to calculate the amplitude of the fundamental and its harmonics. This summation is the square root of the sum of the squares of the amplitude of the cell one below the frequency, the frequency, and the cell one above the frequency. The total harmonic distortion (THD) is calculated as the square root of the sum of the squares of the five harmonics minus the fundamental's amplitude:

$$THD\ (dBc) = \sqrt{A_2^2 + A_3^2 + A_4^2 + A_5^2 + A_6^2} - A_F$$

where A_F is the amplitude of the fundamental and A_2 - A_6 are the amplitudes of the harmonics (using the three cell summation).

The signal-to-noise ratio (SNR) is calculated by taking the square root of the sum of the squares of all cells, excluding cells 0, 1, and 2 (the DC term), the three cells centered around each harmonic, and ten cells centered around the fundamental (to minimize the leakage effects). The signal-to-noise and distortion (SINAD) is calculated the same as the SNR, except that the harmonic cells are included. The SFDR excludes the DC cells (0 - 2) and ±10 cells around the fundamental.

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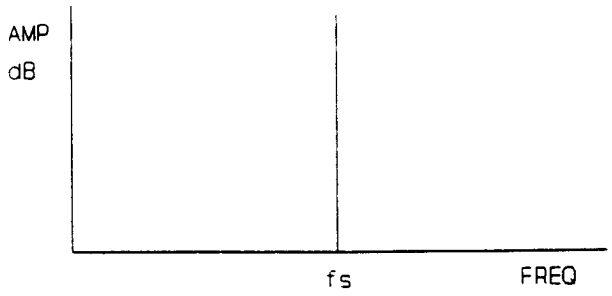
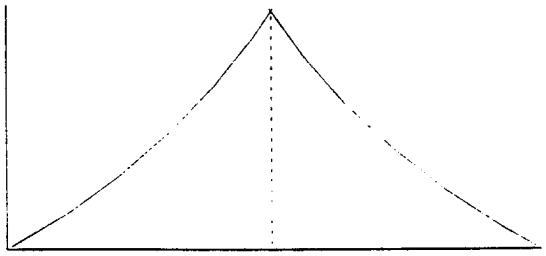
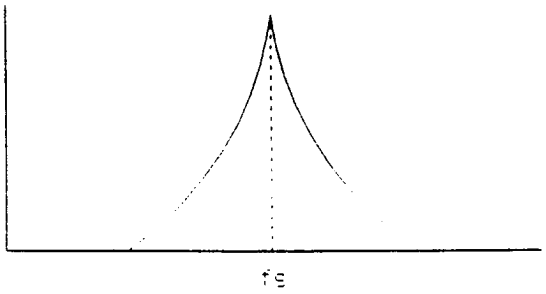


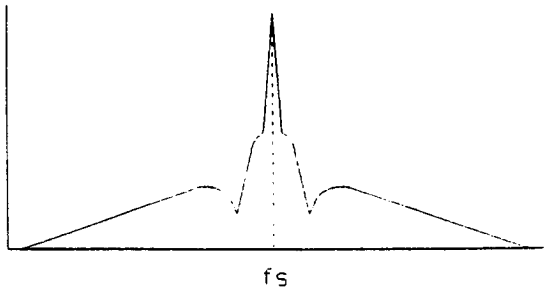
IDEAL SPECTRUM



FFT SHOWING LEAKAGE EFFECTS



FFT USING THE HANNING WINDOW



FFT USING THE BLACMAN HARRIS WINDOW

Figure 11: FFT Spectra

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Appendix F
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

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User-Replaceable Parts

Part Description	Part Number
User Manual	070-9140-XX
Label, Tek CDS	950-0654-00
Label, VXI	950-0944-00
Fuse, Micro 5 Amp 125 V Fast	159-0207-00
Fuse, Micro 2 Amp 125 V Fast	159-0128-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00
Shield, Front	950-1335-00
Screw, Phillips Metric 2.5 × 4 FLHD SS	211-0867-00

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Appendix G
Options

Option 02

Option 02 changes the VX4240 to 1 MSample Memory.

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VX4240 Option 2A (Waveform Output)

The Waveform Output Option allows the digitized input signal that has been captured by the VX4240 to be played back after a programmable delay. The digitized signal is coupled to the Waveform Output Card via the VXI local bus and converted back to an analog signal. A cable connected between the front panel connectors of the two cards enables the output during playback. When playback is not enabled the output is set to zero volts.

When this option is installed, there are changes to the Specifications, Operation, I/O connections, and Calibration.

Specification Changes

Waveform Outputs

Waveform Delay	200 nS to 420 seconds in 200 nS steps
Settling Time	200 nS to 1% (50 ohm load)

10.0 Vpp @50 Ohms Output

Amplitude:	±10.0 Volts ±1% into 1 Megohm ±5.00 Volts into 50 Ohms
Output Impedance	50 Ohms ±5%

1.00 Vpp @50 Ohms Output

Amplitude:	±1.00 Volts ±1% into 1 Megohm ±0.50 Volts into 50 Ohms
Output Impedance	50 Ohms ±1%

Operation Changes

To support Option 2A (Waveform Output), the following trigger commands have been added to the VX4240. These are special purpose commands, and should ONLY be used in conjunction with Option 2A.

Option 2A allows playback of digitized data. The amount of data, and the time the data is played back are both programmable. The D(elay) command specifies the time between the END of sampling data and when playback begins (from 200 nS to 420 seconds, in 200 nS intervals). The 'n' option to these trigger commands specifies how much data is played back. When using these commands, the card must be programmed for the post-trigger (CT) mode. Playback always begins with the oldest data in memory.

To prevent playback of 'old' data in memory, the card internally ANDs the trigger condition specified by the M(ode) command with a soft trigger. Therefore, only one trigger condition can be specified with the mode command. If more than one is specified, the card will override the second condition. When the card receives a TX/TY/TZ trigger command, it first enables sampling of the data. However, before arming the trigger, it will delay the count specified by the collect (CT) command, before the trigger is armed. This guarantees that old data will never be output by the card. Note that the (collect count * sampling period) is added to the trigger rearm time.

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Commands:

TX[n]

This command does a single shot digitization of the input signal. Memory is first zeroed, then the card is armed. After the card has triggered, and memory filled, the programmed delay (D command) is executed. When the delay time has elapsed, the A/D memory is recirculated to drive the Waveform Output card. For the TX command, [n] specifies how many times to playback the data. For [n] <2, the data is played back once, and the card stops. This mode allows the digitized data to be read from the VX4240 after the playback to view/analyze the digitized input. The data is always output beginning at the oldest data in memory, for the full amount of memory on the card. When playing back the data, each playback is separated by the programmed delay time. Because the amount of post-trigger data is programmable (CT command), playback data can include data prior to the trigger (effective pre-trigger data). The front panel display will momentarily show "DACP" indicating the playback trigger has been programmed.

TY[n]
TZ[n]

These two commands are identical, except that the TZ command zeroes memory prior to rearming the trigger. These commands operate the same as the TX command, except they automatically rearm the card after the playback. Playback always begins with the oldest data in memory. For these commands, [n] specifies the amount of data to playback. If [n] is not specified, it defaults to the amount of memory on the card. The greatest value (G) command is inhibited for these two modes. The front panel display will show "DACR" or "DACZ" while the card is in the continuous rearm/playback mode. For the TY command, the rearm time is approximately 100 µS + (collect count * sampling period). For TZ, the rearm time is approximately

100 µS + (RAMsize * 2.25 µS) + (collect count * sampling period).

Example:
As an example, suppose the card were to be triggered by a positive slope crossing at 1.5 volts, and the playback was to include 5000 samples prior to this trigger, delayed by 50 mS from the trigger. The pertinent commands are:

```
CT5000  (collect RAMsize - 5000 samples after the trigger)
M+S1.5  (positive slope trigger at +1.5 volts)
```

Because the playback delay is relative to the end of sampling, there would be a time period of (sampling period * (RAMsize - collect count)) for the card to collect the data. At a period of 100 nS (10 MHz) and 262144 words of memory (with a CT count of 5000), the digitization time is (100e-9 * (262144 - 5000)) or 25.7144 mS.

This implies the delay should be programmed to (50 mS - 25.7114 mS) with the command

```
D24.2856E-3
```

To play back the data, the appropriate trigger command can now be issued. For example, in the continuous rearm mode:

```
TY
```


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Calibration:

Equipment Required:

Function Generator
4½ Digit Voltmeter
Oscilloscope

Procedure:

1. Send the following command to the VX4240-2A

   r;v1;d2e-7;m+s.5;f26e3;tx10

2. Apply a 0.1 Hz, 1mVpp square wave signal from the Function Generator to SIG IN + on the VX4240.

3. Connect the voltmeter to the 10VPP output on the Waveform Output Card.

4. Adjust R741 to 0V ±1mV.

5. Change the amplitude of the function generator to 4VPP.

6. After about 30 seconds the square wave will play back as a plus full scale, minus full scale signal. Adjust R763 for a difference of 19.998V ±10mV between the high and low readings.

7. Change the frequency of the function generator to 1.0MHz.

8. Remove the voltmeter and connect the oscilloscope to the 10VPP output using a 50 ohm load on the scope input.

9. Send the following command to the VX4240-2A

   f1e7;ty

10. Adjust R643 for minimum overshoot on the scope display of the square wave. Ignore the intermediate points that are digitized on the rising and falling edges of the square wave.

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Appendix H: Performance Verification

This procedure verifies the performance of the VX4240 Waveform Digitizer/ Analyzer Module. The verification may be performed in your current VXIbus system if it meets the requirements described in Table A–2. Also, it is not necessary to complete the entire procedure if you are only interested in a certain performance area. However, because some performance parameters depend on the correct operation of previously verified functions, it is recommended that you follow the order presented.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

Please familiarize yourself with the following conventions which apply throughout this procedure:

- Each test sequence begins with a table, similar to the one below, providing information and requirements specific to that section. The item numbers refer to entries in Table A–1, Required Test Equipment. Following the table, you will be given instructions for interconnecting the VX4240-under-test and for checking performance parameters. Test results may then be recorded in the Table A–4, Test Record.

Equipment Requirements	Digital Volt Meter (item 2) Function Generator (item 3)
Prerequisites	All prerequisites listed on page A–40

- This procedure assumes that you will be using the National Instruments PC GPIB controller and software (NI-488.2M), configured as described in Table A–3. In the test sequences you will be instructed to issue Interface Bus Interactive Control (ibic) commands to set up the VX4240-under-test system. Commands to the VX4240 may be entered in upper or lower case. Please refer to the NI-488.2M User Manual for additional information. If you are using a different controller, simply substitute the equivalent commands.

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Prerequisites

The verification sequences in this procedure are valid when the following requirements are met:

- The VX4240 module covers are in place and the module is installed in an approved VXIbus mainframe according to the procedure in the chapter *Getting Started*.
- The VX4240 has passed the self test.
- The VX4240 has been operating for a warm-up period of 10 minutes in an ambient environment as specified in the chapter *Specifications*.

Equipment Required

This procedure uses traceable signal sources and measurement instruments to check performance. Table A–1 lists the required equipment. You may use equipment other than the recommended examples if it meets the minimum requirements listed.

Table A–1: Required Test Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. DC Calibration Generator	Amplitude to ±100V; accuracy to 0.1%	Data Precision 8200	Checking DC accuracy
2. Digital Volt Meter (DVM)	5-1/2 digit, 100 VDC range, AC RMS to 300 kHz, accuracy > 0.002 %.	HP3456A	Checking isolation and voltage accuracy
3. Pattern Generator	25 MHz, TTL, ±10 VDC	Tektronix/CDS VX4750	Checking AC accuracy
4. 50 Ω BNC Coxial Cable (three required)	50 Ω BNC male connectors	Tektronix part number 012-0057-01	Interconnecting electrical signals
5. BNC-T Connector (two required)	50 Ω impedance; BNC female to BNC female to BNC male	Tektronix part number 103-0030-00	Interconnecting electrical signals
6. BNC Female to Dual Banana	50 Ω impedance; BNC female, Dual Banana plug	Tektronix part number 103-0090-00	Interconnecting electrical signals

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VX4240-Under-Test Configuration

To execute this procedure, the VX4240-under-test must be installed in an approved VXIbus system. Minimally, this system must contain the elements listed in Table A–2.

Table A–2: Elements of a Minimum VX4240 -under-test System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	Two available slots in addition to the Slot 0 controller, for the VX4240 and a Pattern Generator	Tektronix VX1400A, VX1410	Power, cooling, and backplane for VXIbus modules
2. Slot 0 Resource Manager	Slot 0 Functions, Resource Mgr., IEEE 488 GPIB Interface	VX4521 Slot 0 Resource Mgr.	Resource Mgr., Slot 0 Functions, GPIB Interface
3. System Controller	286 Processor; GPIB card and Software,Talker/Listener/Controller	IBM 486 PC, National Insruments GPIB PC2A card & NI-488.2M software	System Controller
4. GPIB Cable	≈2 m length, GPIB connectors	Tektronix part number 012–0991-00	Connecting PC GPIB to Slot 0
5. VX4240-Under-Test	Not applicable	Not applicable	Verify its performance

Test System Configuration

Table A–3 describes the VXIbus system configuration assumed in this procedure. If your configuration is different, you do not need to change it, just note that you will observe your device names and addresses in the test sequences. (Note that no secondary addressing is assumed.)

Table A–3: VXIbus Test System Configuration (Assumed)

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address	GPIB Primary Address
GPIB0	GPIB0	(PC card)	NA	30
VX4521	VX4521	Slot 0	13 (0D hex)	13
VX4240 -under-test	VX4240	Slot 1	01	1
VX4750	VX4750	Slot 2	02	2

Test Record

Photocopy the Test Record, and use it to record the performance verification results for your module.

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Table A–4: VX4240 Test Record

VX4240 Serial Number:	Temperature and Relative Humidity:
Date of Last Calibration:	Verification Performed by:
Certificate Number:	Date of Verification:

VXIbus Interface		**Logical Address, IEEE Address, Slot No., MFG., Model, etc.**	
Table Command Response (System Configuration)	1st. Response		
	2nd Response		
	3rd Response		
		Passed	**Failed**
Program Command Response	Extended Self Test		
	Interrupt SRQ		
Common Mode Rejection	CMRR		

DC Voltage Accuracy [1]						
0.5 V Range (0.4% full scale or ±4 mV)	**DC Calibrator**	0.490 V	0.250 V	0.000 V	–0.250 V	–0.490 V
	Max.	0.494 V	0.254 V	0.004 V	–0.246 V	–0.486 V
	Measure					
	Min.	0.486 V	0.246 V	–0.004 V	–0.254 V	–0.494 V
1 V Range (0.2% full scale or ±4 mV)	**DC Calibrator**	0.9000 V	0.5000 V	0.000 V	–0.500 V	–0.9000 V
	Max.	0.9040 V	0.5040 V	0.004 V	–0.496 V	–0.8960 V
	Measure					
	Min.	0.8960 V	0.4960 V	–0.004 V	–0.504 V	–0.9040 V
2 V Range (0.2% full scale or ±8 mV)	**DC Calibrator**	1.9000 V	1.0000 V	0.000 V	–1.000 V	–1.9000 V
	Max.	1.9080 V	1.0040 V	0.008 V	–0.992 V	–1.8920 V
	Measure					
	Min.	1.8920 V	0.9960 V	–0.008 V	–1.008 V	–1.9080 V
5 V Range (0.2% full scale or ±20 mV)	**DC Calibrator**	4.9000 V	2.5000 V	0.000 V	–2.500 V	–4.9000 V
	Max.	4.9200 V	2.5200 V	0.020 V	–2.480 V	–4.8800 V
	Measure					
	Min.	4.8800 V	2.4800 V	–0.020 V	–2.520 V	–4.9200 V

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DC Voltage Accuracy (Cont.)[1]						
10 V Range (0.2% full scale or ±40 mV)	**DC Calibrator**	9.9000 V	5.0000 V	0.000 V	–5.000 V	–9.9000 V
	Max.	9.9400 V	5.0400 V	0.040 V	–4.960 V	– 9.8600 V
	Measure					
	Min.	9.8600 V	4.9600 V	–0.040 V	–5.040 V	–9.9400 V
20 V Range (0.2% full scale or ±80 mV)	**Voltage**	19.000 V	10.000 V	0.000 V	–10.00 V	–19.000 V
	Max.	19.080 V	10.080 V	0.080 V	–9.920 V	–18.920 V
	Measure					
	Min.	18.920 V	9.9200 V	–0.080 V	–10.80 V	–19.080 V
50 V Range (0.2% full scale or ±200 mV)	**DC Calibrator**	49.000 V	25.000 V	0.000 V	–25.00 V	–49.000 V
	Max.	49.200 V	25.200 V	0.200 V	–24.80 V	–48.800 V
	Measure					
	Min.	48.800 V	24.800 V	–0.200 V	–25.20 V	–49.200 V
100 V Range (0.2% full scale or ±400 mV)	**DC Calibrator**	99.000 V	50.000 V	0.000 V	–50.00 V	–99.000 V
	Max.	99.400 V	50.400 V	0.400 V	–49.60 V	– 98.600 V
	Measure					
	Min.	98.600 V	49.600 V	–0.400 V	–50.40 V	–99.400 V

1 **Add Temperature Drift: <0.03% of full scale 1° C (all ranges).**

AC Voltage Accuracy		1 kHz	10 kHz	100 kHz
3.464 V_{RMS}	**Max.**			
	Measure			
	Min.			
7.070 V_{RMS}	**Max.**			
	Measure			
	Min.			

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Self Test

The VX4240 includes a built-in self test feature (BITE) which is executed automatically at power-on and (more extensively) when the Self Test command (S) is issued. Internal test routines and reference circuitry verify the CPU, RAM, A/D converter, and the analog input amplifiers. Parameters tested include common mode, coupling, offset, and range gain. No external test equipment is required .

In addition to BITE, two of the front panel indicator lights display the current status of power and the SYSFAIL* error condition. The front-panel alphanumeric display will show error codes due to a hardware failure or incorrect programming. The error command (E), may be used at any time during operation to determine the current state of the module.

Following the system initialization the front panel will normally display RDY and the green PWR light will be on indicating that the self test has passed and that the power supplies are operational. If the +5 V, ±24 V (including the derived ±15 V), –5.2 V, or –2 V power supplies fail, or if a corresponding fuse opens, the PWR light will be off and the red FAILED light will be on (indicating that SYSFAIL* has been asserted due to a failure).

NOTE. *If you experience an error indication from the Slot 0 Resource Manager, the VX4240-under-test, or other VXIbus module, investigate and correct the problem before proceeding. Common items to check are logical address conflicts (primary and secondary; see Table A–3), breaks in the VXIbus daisy chain signals, improper seating of a module, loose GPIB cable, improperly set Slot 0 single step switch, or loose or blown fuses.*

Performance Verification Tests

This procedure contains instructions for the example test equipment listed in Table A–1. You may use instrumentation other than the recommended example if it meets the minimum requirements listed. The order of execution has been chosen to minimize system setup and programming requirements. Although not essential, it is recommended that you follow the order presented, as some tests rely on previously verified parameters.

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VXIbus Interface

This sequence verifies that the VX4240 configures correctly and communicates properly with your GPIB system controller.

Equipment Requirements	No additional test equipment is required for this sequence.
Prerequisites	All prerequisites listed on page A–40

1. To verify the system configuration, send the TABLE command to the Slot 0 Resource Manager and confirm the responses shown in table A–5. Your configuration may not be identical, but the responses should be similar. (If you are using a controller other than the VX4521, use the equivalent procedure to observe the system configuration.)

Table A–5: VXIbus System Configuration

Command to Type	Response to Verify
`ibic`	
`ibfind VX4521`	
`ibwrt "table"`	
`ibrd 200`	`03`
`!`	`LA 0, IEEE 13, Slot 0, MFG FFDh, MODEL VX4521, PASS, , RM..`
`!`	`LA 1, IEEE 01, Slot 1, MFG FFCh, MODEL VX4240, PASS TRIGGER;LOCK;READ STB, MESG, 0, V1.3, NORMAL`
`!`	`LA 2, IEEE 02, Slot 2, MFG FFDh, MODEL VX4750, PASS TRIGGER;LOCK;READ STB, MESG, 0, V1.3, NORMAL`

NOTE. *If you are using National Instruments NI-488.2 software you may wish to select the* `buffer 1` *mode to allow more comfortable viewing of the ASCII response. Just type* `buffer 1.`

2. With the following commands, perform an extended self test and verify that there are no pending errors:

```
ibfind VX4240

ibwrt "s\n"
```

(Observe status messages on front panel and then RDY)

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```
ibrd 100
```
(Observe S00000.., see Query command 3-79)

3. Verify the VX4240 VXIbus interrupt capability with the following steps:

NOTE*. Make sure your Slot 0 controller and the VX4240-under-test are set to the same interrupt level. Also, if you are using National Instruments NI-488.2 software, make sure Auto Serial Polling is disabled to prevent the SRQ from being reset prior to a visual check.*

a. Set the VX4240 to its power-on default state, enable VXIbus Request True Backplane interrupt (due to a triggered condition), assert a trigger, and read the result:

```
ibwrt "r;bt;t\n"
```
(Observe RFI, TRG and MC lights on)

```
ibrd 100
```
(Observe S00011 response and VX4521 indicates S)

b. Check that the RFI light is now off, the TRG and MC lights are on, and that the Slot 0 controller (VX4521) displays an S for an SRQ pending. The response S00011 indicates that the Acquisition memory is full and that Real Time data has been updated (see Query command 3-79).

NOTE*. The read command serves to unaddress the Slot 0 controller allowing it to detect the VXIbus interrupt and to assert the SRQ.*

c. Perform a Serial Poll of the VX4240 and verify an F9 (hex) response (indicating an IRQ due to trigger) and that the Slot 0 SRQ is no longer asserted.

```
ibrsp
```
(Observe F9 response and VX4521 no longer displays S.)

Common Mode Rejection

This sequence verifies a Common Mode Rejection Ratio (CMRR) of better than 100:1 (>40 dB, DC to 1 kHz).

Equipment Requirements	VX4750 (item 3) DVM (item 2) 50 Ω BNC cable, three required (item 4) BNC-T adaptor, two required (item 5) BNC to Dual Banana (item 6)
Prerequisites	All prerequisites listed on page A–40

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1. Connect the VX4750 FUNC OUT signal to the DVM and to the VX4240 SIG IN+ and SIG IN– inputs with the following steps:

   a. Connect a BNC-to-Dual Banana adaptor and a BNC-T connector to the DVM input.

   b. Connect the VX4750 FUNC OUT signal to one side of the BNC-T.

   c. Using equal length coxial cables and a second BNC-T, connect the VX4240 SIG IN+ and SIG IN– inputs to the other side of the BNC-T at the DVM.

2. Set the VX4750 to its power-on default, for a 1 MΩ output impedance, and to generate a 1 kHz, 9.8 V_{p-p} sine wave:

   ```
   ibfind VX4750

   ibwrt "rst;imp 1e6;ampl 9.8vpp;freq 1e3"
   ```

3. Set the VX4240 to its power-on default state, for a single-ended 5 V range with a 1 MΩ input impedance, to trigger an acquisition, and then to analyze and read back the true RMS value:

   ```
   set VX4240

   ibwrt "r;v5ms;t\n"

   ibwrt "at\n"

   ibrd 100
   ```
   (Record the RMS value returned as V_s)

4. Set the VX4240 to repeat the acquisition in differential mode and then to analyze and read back the true RMS value:

   ```
   ibwrt "r;v5md;t\n"

   ibwrt "at\n"

   ibrd 100
   ```
   (Record the RMS value returned as Vd)

5. Calculate the CMRR = 20Log_{10} (Vs/Vd) and verify the result to be greater than 40 dB.

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DC Voltage Accuracy

This sequence verifies the DC accuracy of the A/D converter and the input attenuator.

Equipment Requirements	DC Calibration Generator (item 1) 50 Ω BNC cable (item 4) BNC to Dual Banana Plug (item 6)
Prerequisites	All prerequisites listed on page A–40

1. Connect the DC Calibrator to the VX4240 SIG IN + input using a BNC cable and a BNC to dual Banana adaptor. Set the DC Calibrator to 0.49 V.
2. With the commands below, set the VX4240 to its power-on state, select the 0.5 V range, and trigger an acquisition. Then perform an Average Analysis and verify the accuracy of the result to be within ±0.4% of the full scale range (±4 mV).

   ```
   set VX4240
   ```

   ```
   ibwrt "r;v0.5;t\n"
   ```
   (Observe TRG and MC lights on)

   ```
   ibwrt "aa\n"
   ```
   (Observe BUSY then RDY on front panel)

   ```
   ibrd 100
   ```
   (Observe: 0.49 V_{DC} ±4 mV)
3. Check the additional voltages listed in Table A–6. Wait for the RDY display before sending the Average Analysis (aa) command.

Table A–6: 0.5 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+0.49000
(step 2 repeated for continuity)
	`ibwrt "r;v0.5;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		0.486 to 0.494 VDC

+0.25000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		0.246 to 0.254 VDC

+0.00000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.004 to +0.004 VDC

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Table A–6: 0.5 V Range Verification (Cont.)

Set DC Calibrator	Command To Send	DC Voltage to Verify

–0.25000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.254 to –0.246 VDC

–0.49000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.494 to –0.486 VDC

4. Check the 1.0 V range listed in Table A–7. Verify the voltages to be within 0.4% of the full scale range (±4 mV).

Table A–7: 1 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+0.90000	`ibwrt "r;v1;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		0.8960 to 0.9040 VDC

+0.50000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		0.496 to 0.504 VDC

+0.00000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.004 to +0.004 VDC

–0.50000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.504 to –0.496 VDC

–0.9000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.9040 to –0.8960 VDC

5. Check the 2.0 V range listed in Table A–8. Verify the voltages to be within 0.2% of the full scale range (±8 mV).

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Table A–8: 2 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+1.90000	`ibwrt "r;v2;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		1.8920 to 1.9080 VDC

+1.00000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		0.992 to 1.008 VDC

+0.00000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.008 to +0.008 VDC

–1.00000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–1.008 to –0.992 VDC

–1.9000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–1.9080 to –1.8920 VDC

6. Check the 5.0 V range listed in Table A–9. Verify the voltages to be within 0.2% of the full scale range (±20 mV).

Table A–9: 5 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+4.90000	`ibwrt "r;v5;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		4.8800 to 4.9200 VDC

+2.50000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		2.480 to 2.520 VDC

+0.00000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.020 to +0.020 VDC

–2.50000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–2.520 to –2.480 VDC

–4.90000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–4.9200 to –4.8800 VDC

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7. Check the 10.0 V range listed in Table A–10. Verify the voltages to be within 0.2% of the full scale range (±40 mV).

Table A–10: 10 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+9.90000	`ibwrt "r;v10;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		9.8600 to 9.9400 VDC

+5.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		4.960 to 5.040 VDC

+0.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.040 to +0.040 VDC

–5.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–5.040 to –4.960 VDC

–9.90000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–9.9400 to –9.8600 VDC

8. Check the 20.0 V range listed in Table A–11. Verify the voltages to be within 0.2% of the full scale range (±80 mV).

Table A–11: 20 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+19.0000	`ibwrt "r;v20;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		18.920 to 19.080 VDC

+10.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		9.9200 to 10.080 VDC

+0.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.080 to +0.080 VDC

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Table A–11: 20 V Range Verification (Cont.)

Set DC Calibrator	Command To Send	DC Voltage to Verify

–10.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–10.080 to –9.9200 VDC

–19.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–19.080 to –18.920 VDC

9. Check the 50.0 V range listed in Table A–12. Verify the voltages to be within 0.2% of the full scale range (±200 mV).

Table A–12: 50 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+49.0000	`ibwrt "r;v50;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		48.800 to 49.200 VDC

+25.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		24.800 to 25.200 VDC

+00.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.200 to +0.200 VDC

–25.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–25.200 to –24.800 VDC

–49.0000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–49.200 to –48.800 VDC

10. Check the 100.0 V range listed in Table A–13. Verify the voltages to be within 0.2% of the full scale range (±400 mV).

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Table A–13: 100 V Range Verification

Set DC Calibrator	Command To Send	DC Voltage to Verify

+99.000	`ibwrt "r;v100;t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		98.600 to 99.400 VDC

+50.000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		49.600 to 50.400 VDC

+00.000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–0.400 to +0.400 VDC

–50.000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–50.400 to –49.600 VDC

–99.000	`ibwrt "t\n"`
	`ibwrt "aa\n"`
	`ibrd 100`
		–99.400 to –98.600 VDC

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AC Accuracy

This sequence verifies the AC RMS accuracy of the VX4240.

Equipment Requirements	Function Generator, VX4750 (item 3) DVM (item 2) BNC-T adaptor, (item 5) 50 Ω BNC cable, two required (item 4) BNC to Dual Banana adaptor (item 6)
Prerequisites	All prerequisites listed on page A–40

1. Connect the VX4750 to the VX4240 SIG IN+ and the DVM using a BNC-T (connected to the VX4750 FUNC OUT signal), two coxial cables, and a BNC to Dual Banana adaptor (connected to the DVM input). Set the DVM to measure AC RMS.

2. Set the VX4750 to its power-on default, and then for a 1 MΩ output impedance and to generate a 1 kHz, 3.464 V_{RMS} sine wave:

   ```
   set VX4750

   ibwrt "rst;imp 1e6;freq 1kHz;ampl 3.464vrms"
   ```

3. Allow a minute for the VX4750 to stabilize and then readjust its output voltage. For example if the DVM indicates 3.578, reset the VX4750 amplitude to 3.464 – (3.578 – 3.464) = 3.350 with the following command (Repeat adjustment until the DVM reads 3.464 V_{RMS} ±0.004 V_{RMS}):

   ```
   ibwrt "ampl 3.350vrms"
   ```
   (Readjust for 3.464 V_{RMS} ±0.004 V_{RMS})

4. With the commands below, reset the VX4240 to its power-on state, select the 5 V range with a 1 MΩ input impedance, and assert a trigger. When the front panel displays RDY, perform a True RMS analysis and read the results. Verify the accuracy to be within 3% of the reading on the DVM.

   ```
   set VX4240

   ibwrt "r;v5m;t\n"
   ```
   (Observe RDY)

   ```
   ibwrt "at\n"
   ```
   (Observe RDY)

   ```
   ibrd 100
   ```
   (Verify with DVM)

5. Reset the the pattern generator and VX4240 and verify the additional voltages and frequencies as instructed in Table A–13 to be within 3.0% of the reading on the DVM.

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Table A–14: AC RMS Verification

Commands to VX4750	Commands to VX4240	AC Voltage to Verify

set vx4750
ibwrt “freq 10 kHz”
	`set vx4240`
	`ibwrt "t\n"`
	`ibwrt "at\n"`
	`ibrd 100`
		DVM reading ±3.0 %

set vx4750
ibwrt “freq 100 kHz”
	`set vx4240`
	`ibwrt "t\n"`
	`ibwrt "at\n"`
	`ibrd 100`
		DVM reading ±3.0 %

set vx4750
ibwrt “Ampl 7.07vrms;freq 1 kHz”
	`set VX4240`
	`ibwrt "v10;t\n"`
	`ibwrt "at\n"`
	`ibrd 100`
		DVM reading ±3.0 %

set vx4750
ibwrt “Freq 10 kHz”
	`set VX4240`
	`ibwrt "t\n"`
	`ibwrt "at\n"`
	`ibrd 100`
		DVM reading ±3.0 %

set vx4750
ibwrt “Freq 100 kHz”
	`set VX4240`
	`ibwrt "t\n"`
	`ibwrt "at\n"`
	`ibrd 100`
		DVM reading ±3.0 %

This completes the VX4240 verification procedure.

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WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

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Appendix I: Adjustment Procedure

In order to meet its published specification, the VX4240 must be adjusted every twelve months. The adjustment should be performed at the temperature at which the module will be operating. If this is not feasible, or the module will be operating over a wide temperature variation, consult the temperature drift specification in the Operating Manual.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

This procedure assumes a system configuration as described in Table A–17 and that you will be using the National Instruments PC-GPIB controller and software (NI-488.2M). The adjustment sequences instruct you to issue the corresponding Interface Bus Interactive Control (ibic) commands to set up the VX4240 and other associated VXIbus test instruments. Please refer to the NI-488.2M User Manual for additional information. If you are using a different controller, simply substitute the equivalent commands in the adjustment steps.

Prerequisites

Proper adjustment of the VX4240 may be achieved when the following requirements are met:

- The VX4240 module covers are in place and the module is installed in an approved VXIbus mainframe according to the procedures in Section 2 of the Operating Manual (The module may be operated on an extender board to allow access to the adjustments)
- The VX4240 has passed its self test
- The VX4240 is operating in an ambient temperature between 0° C and +55° C and has been operating for a warm-up period of 10 minutes

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Equipment Required

This procedure uses traceable signal sources and measurement instruments. Table A–15 lists the required equipment. You may use equipment other than the recommended examples if it meets the minimum requirements listed.

Table A–15: Required Adjustment Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. DC Calibration Generator	Variable amplitude to ±100V; accuracy to 0.1%	Data Precision 8200	Adjusting DC accuracy
2. Sine Wave Generator	1 MHz, 7.07 V_{RMS} ± 0.004 V_{RMS}	Tektronix/CDS VX4750	Adjusting AC accuracy
3. Digital Volt Meter (DVM)	5-1/2 digit, 100 VDC range, accuracy > 0.002 %.	FLUKE 8842A	Checking voltage accuracy
4. VXIbus Extender Board	Full length extension of C size VXIbus	Tektronix/CDS 73A–850	Providing adjustments access
5. BNC-T, (two required)	50 Ω impedance; BNC female to BNC female to BNC male	Tektronix part number 103-0030-00	Interconnect electrical signals
6. BNC Female to Dual Banana	50 Ω impedance; BNC female to Dual Banana	Tektronix part number 103-0090-00	Interconnect electrical signals
7. 50 Ω BNC Coxial Cable (three required)	50 Ω impedance; BNC male connectors	Tektronix part number 012-0057-01	Interconnect electrical signals

System Requirements

In order to perform this procedure, the VX4240 must be installed in an approved VXIbus system. At a minimum, the system must contain the elements listed in Table A–16.

Table A–16: Elements of a Minimum VX4240 Adjustment System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	Two available slots, for the VX4240 and the Pattern Generator in addition to the Slot 0 controller	Tektronix VX1400A	Power, cooling, and backplane for VXIbus modules
2. Slot 0 Controller	Resource Mgr., Slot 0 Functions, IEEE 488 GPIB Interface	VX4521 Slot 0 Resource Mgr.	Slot 0 functions, Resource Mgr., and GPIB-VXIbus interface
3. IBM PC or compatible	286 Processor; Talker/Listener/ Controller GPIB card, and software	IBM 486 PC, National Insruments GPIB PC2A card & NI-488.2M software	System Controller

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Table A–16: Elements of a Minimum VX4240 Adjustment System (Cont.)

Item Number and Description	Minimum Requirements	Example	Purpose
4. GPIB Cable	≈ 2 m length, GPIB connectors on each end	Tektronix part number 0120–0991-00	Connecting PC-GPIB to Slot 0
5. VX4240 on extender board	Not applicable	Not applicable	Adjustment

System Configuration

Table A–17 describes the VXIbus system configuration which is assumed in this procedure. If your configuration is different, you do not need to change it, just note that you will observe your device names and addresses in place of those recommended in table A–17.

Table A–17: VXIbus Adjustment System Configuration

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address	GPIB Primary Address
GPIB0	GPIB0	(PC card)	NA	30
VX4521	VX4521	Slot 0	00	13
VX4240 on extender	VX4240	Slot 1	01	1
VX4750	VX4750	Slot 2	02	2

Adjustment Procedure

The following sequences reestablish internally stored adjustment parameters and adjust AC and DC offset imbalance in the differential input signal paths. The steps must be followed in the order presented to ensure adjustment parameter interdependencies. Refer to Figure 12 for the location of module adjustments.

NOTE. *If you are using National Instruments NI-488.2 software you may wish to select the buffer 1 display mode to allow more comfortable viewing of the ASCII response (Just type* `buffer 1`*).*

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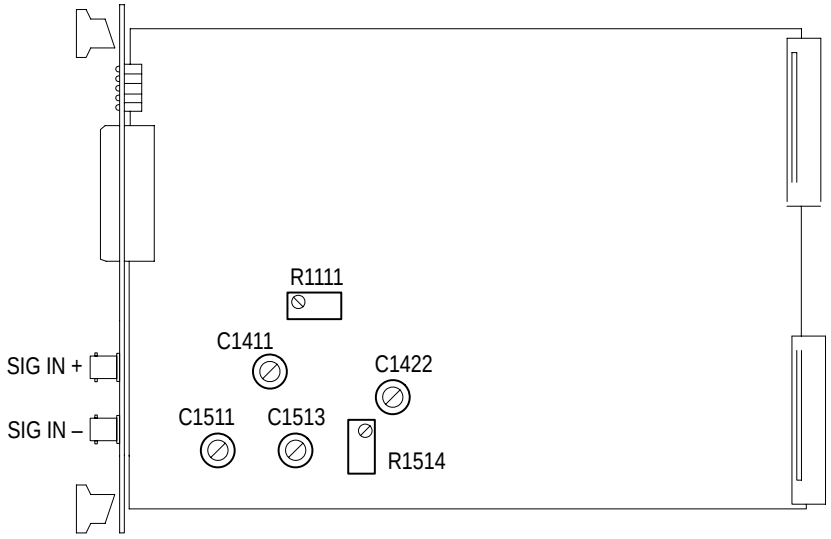

Figure 12: VX4240 Adjustment Locations

DC Common Mode Adjustment

This sequence first adjusts the DC gain and input signal path imbalances for the 0.5 V and 5.0 V ranges and then adjusts for maximum common mode rejection. New adjustment constants are stored in non-volatile memory.

1. Connect the DC Calibrator to the VX4240 SIG IN+ and SIG IN– using equal length coxial cables, a BNC-T, and a BNC-to-Dual Banana adaptor.
2. Set the DC Calibrator for +0.49000 V_{DC}.
3. Set the VX4240 to auto-adjust DC gain and offset for the 0.5 V range (Note: While the auto-adjustment is converging, the front panel will display hexadecimal values and when complete, will display RDY):

   ```
   ibfind VX4240

   ibwrt "ks0.5\n"
   ```
   (Observe hex values and then RDY)
4. Set the VX4240 to display the differential input voltage for the 0.5 V range, and while observing the front panel display, adjust R1111 for the closest reading to 0.0 (±15.0 maximum):

   ```
   ibwrt "kz0.5\n"
   ```
   (Observe display and adjust R1111)
5. Repeat steps 3 and 4 until no additional adjustment is required in step 4.
6. Set the DC Calibrator for +4.90000 V_{DC}.

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7. Set the VX4240 to auto-adjust DC gain and offset for the 5.0 V range:

   ibwrt ”ks5\n”
   (Observe hex values and then the RDY)

8. Set the VX4240 to display the differential voltage for the 5.0 V range, and while observing the front panel display, adjust R1514 for the closest reading to 0.0 (± 15.0 maximum):

   ```
   ibwrt "kz5\n"
   ```
   (Observe display and adjust R1514)

9. Repeat steps 7 and 8 until no additional adjustment is required in step 8.

DC Gain and Offset Adjustment

This sequence auto-adjusts the DC gain and balances the differential offset for all eight voltage ranges. New adjustment constants are stored in non-volatile memory. While the auto-adjustment is converging, the front panel will display changing hexadecimal values. When the command is complete, the module will display RDY, indicating that the next range may be adjusted. If the module does not converge for a specified range, the display will indicate an error number. The Error command (E) may be used to read the cause of the failure. This usually occurs if an incorrect voltage has been set up for the range being adjusted.

1. Connect the DC Calibrator to the VX4240 SIG IN+ input only, using a coaxial cable and a BNC-to-Dual Banana adaptor.

2. As specified in Table A–18, adjust the eight voltage ranges by setting the DC Calibrator and sending the auto-adjustment command for each calibrator setting according to Table A–18.

3. When RDY appears on the display after each auto-adjustment command, reverse the polarity of the calibrator voltage and read the negative voltage using the following commands:

   ibwrt “R;CT10002;VD#;TF\n”
   (substitute the # with the voltage range 0.5, 1, 2...etc.)

   ibwrt “AA10000/0\n”

   ibrd = measured negative voltage

4. Calculate the new calibration voltage with the following equation:

   New cal. voltage = [-(cal.voltage) - (measured negative voltage)]/2 + cal. voltage

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5. Set the calibrator to the new calibration voltage and send the autoadjustment command according to Table A–18.

Example: To set DC gain and offset in the 2V range, do the following:

1. Set the DC calibrator to +1.96V.
2. Send the command “ks2\n” and wait for RDY to appear in the display.
3. Set the DC calibrator to –1.96V.
4. Send the command “R;CT10002;VD2;TF\n”.
5. Send the command “AA10000/0\n”.
6. Read the VX4240 and get the measured negative voltage.
7. Use the voltage measured in step 6 and the following equation to calculate the new calibration voltage.

   Example:

   $$1.964695 = [-1.96 - (-1.96939)] /2 + 1.96$$

8. Set the DC calibrator to +1.964695V.
9. Send the command “ks2\n” and wait for RDY to appear on the display and proceed to the next range.

Table A–18: DC Gain and Offset Adjustment

Set DC Calibrator	Command To Send	Range Adjusted
+0.49000	`ibwrt "ks0.5\n"`	0.5 V
+0.98000	`ibwrt "ks1\n"`	1.0 V
+1.96000	`ibwrt "ks2\n"`	2.0 V
+4.90000	`ibwrt "ks5\n"`	5.0 V
+9.80000	`ibwrt "ks10\n"`	10.0 V
+19.6000	`ibwrt "ks20\n"`	20.0 V
+49.0000	`ibwrt "ks50\n"`	50.0 V
+98.0000	`ibwrt "ks100\n"`	100.0 V

AC Gain and Common Mode Adjustment

This sequence adjusts the single-ended AC gain and the maximum AC common mode rejection of the upper ranges (5 and 50 VAC). The reference signal is

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produced by a 100 kHz sine wave generator which is set to a precise voltage using a DVM.

1. Connect the VX4750 FUNC OUT signal to the DVM and to the VX4240 SIG IN+ and SIG IN– inputs with the following steps:

   a. Connect a BNC-to-Dual Banana adaptor and a BNC-T connector to the DVM input.

   b. Connect the VX4750 FUNC OUT signal to one side of the BNC-T.

   c. Using equal length coxial cables and a second BNC-T, connect the VX4240 SIG IN+ and SIG IN– inputs to the other side of the BNC-T at the DVM.

2. Set the VX4750 to its power-on default, and then for a 1 MΩ output impedance, and to generate a 100 kHz, 3.464 V_{RMS} sine wave:

   ```
   set VX4750

   ibwrt "rst;imp 1e6;ampl 3.464vrms;freq 100e3"
   ```

3. Allow a minute for the VX4750 to stabilize and then readjust its output voltage. For example if the DVM indicates 3.578, reset the VX4750 amplitude to 3.464 – (3.578 – 3.464) = 3.350 with the following command (Repeat until the DVM reads 3.464 V_{RMS} ±0.004 V_{RMS}):

   ```
   ibwrt "ampl 3.350vrms"
   ```
   (Readjust for 3.464 V_{RMS} ±0.004 V_{RMS})

4. Momentarily disconnect the coxial cable from the VX4240 SIG IN– input.

5. Using the commands which follow, set the VX4240 to display the RMS input voltage for the 5.0 V range and while observing the front panel display, adjust C1411 for the closest reading to 3464 ±10:

NOTE. *Very small adjustments will cause large changes in the display.*

   ```
   set VX4240

   ibwrt "ka5\n"
   ```
   (Adjust C1411 for 3464 ±10)

6. Reconnect the coaxial cable to the VX4240 SIG– input.

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7. Set the VX4240 to display the Common Mode input voltage for the 5 V range and while observing the front panel display, adjust C1511 for the minimum count possible < 75:

   ```
   ibwrt "kd5\n"
   ```
   (Adjust C1511 for minimum count < 75)

8. Momentarily disconnect the coxial cable from the VX4240 SIG IN– input.

9. Repeat step 5 and readjust if necessary.

10. Reset the VX4750 amplitude to 7.07 V_{RMS} and then readjust its output voltage. For example if the DVM indicates 7.25, reset the VX4750 amplitude to 7.07 – (7.25 – 7.07) = 6.890 (Repeat until the DVM reads 7.070 V_{RMS} ±0.004 V_{RMS}):

    ```
    set VX4750

    ibwrt "ampl 7.07vrms"

    ibwrt "ampl 6.890vrms"
    ```
    (Readjust for 7.070 V_{RMS} ±0.004 V_{RMS})

11. Set the VX4240 to display the RMS input voltage for the 50 V range and while observing the front panel display, adjust C1422 for the closest reading to 7070 ±20:

    ```
    set VX4240

    ibwrt "ka50\n"
    ```
    (Adjust C1422 for 7070 ±20)

12. Reconnect the coaxial cable to the VX4240 SIG– input.

13. Set the VX4240 to display the Common Mode input voltage for the 50 V range and while observing the front panel display, adjust C1513 for the minimum count possible < 350:

    ```
    ibwrt "kd50\n"
    ```
    (Adjust C1513 for minimum count < 350)

14. Disconnect the cable from the VX4240 SIG– input and repeat step 11.

15. Reset the VX4240 to its power-on default state:

    ```
    ibwrt "r\n"
    ```

    This completes the VX4240 adjustment procedure.

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Appendix J: Binary Transfer

If you are using a National Instruments GPIB-VXI/C Slot 0 module and are planning on using the binary transfer capabilities of the modules above, you will need to load a CI (Code Instrument) into the GPIB-VXI/C Slot 0.

NOTE. *The GPIB-VXI/C Slot0 has an internal buffer that holds the data to be read out. The buffer will automatically take a reading from the module upon a GPIB read. The buffer will read the module until it receives an END BIT (bit 8 set in the response to a byte request command). The Tektronix products above do not set bit 8 on readback, thus the GPIB-VXI/C Slot0 will fill its buffer with data (approximately 450 Kbytes). If you only request 1 Kbytes of data over GPIB there still will be 449 Kbytes of data in the buffer. This data will remain in the buffer until read out. If you should request data from another module the data that you will receive back will be from the data that is left over in the buffer (449 Kbytes).*

National Instruments has developed a code instrument that will read the exact number of bytes that was requested over the GPIB bus from the module. The code instrument will not read more data then requested and will have no leftover data in the buffer. Refer to the National Instruments GPIB-VXI/C manual for information on code instruments.

If you need any assistance call 1-800-TEK-WIDE or contact your local Tektronix representative.

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Appendix K: IEEE-488 Address

If you are using a National Instruments GPIB-VXI/C Slot 0 module, you may have trouble attaining an IEEE-488 address for the VX4240. When the system is powered on the GPIB-VXI/C Slot 0 resource manager does not assign a GPIB address because the RESMAN delay is too short to allow the VX4240 to perform its self test. To correct the problem change the RESMAN delay when you power on to set the GPIB-VXI/C Slot 0 nonvolatile memory.

Perform the following steps:

1. Connect an RS-232 cable to the GPIB-VXI/C Slot 0 serial port and the opposite end to a terminal. (Refer to the National Instruments User manual.)
2. Power on the GPIB-VXI/C Slot 0. The following information should appear on the screen.

```
GPIB–VXI>
```

3. Type in CONF and press enter. The following information should appear on the screen.

```
GPIB–VXI>CONF
```

4. The following information should appear on the screen.

```
GPIB–VXI Nonvolatile Configuration Main Menu

      (C) 1995  National Instruments

================================================

   1). Read In Nonvolatile Configuration

   2). Print Configuration Information

   3). Change Configuration Information

   4). Set Configuration to Factory Settings

   5). Write Back (Save) Changes

   6). Quit Configuration

   Choice (1–6):
```

5. Type in 1 and press return. The following information should appear on the screen.

```
Reading in Nonvolatile Configuration....Done!
```


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```
<<Press A Key to Return to Main Menu>>
```

6. Press the space bar and the following information should appear on the screen.

```
GPIB–VXI Nonvolatile Configuration Main Menu

          (C) 1995  National Instruments

   ================================================

   1). Read In Nonvolatile Configuration

   2). Print Configuration Information

   3). Change Configuration Information

   4). Set Configuration to Factory Settings

   5). Write Back (Save) Changes

   6). Quit Configuration

   Choice (1–6):
```

7. Enter a 2 and press return. The following information should appear on the screen.

```
====== Nonvolatile Configuration Information =======

Logical Address: 0x00             Device Type    :
Message Based

Manufacturer Id: 0xFF6            Model Code     :
0x0FF (Slot 0)

Slave Addr Spc : A24              Protocol Reg   :
0x0FF0

RESET Config   : PBtoLocalRESET PBtoSYSRESET SYSRE-
SETtoLocalRESET

Serial Number  : 0x00011054

Region 1 Size  : 0x070000         Number Procs   :
0x20

Number Exchgs  : 0x20
Number Msgs    : 0x180

Console: Enabled
RM Wait period : 0 seconds
```


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```
VXI Interrupt Level To Handler Logical Address (0xFF
= free to assign):

  1:0xFF,  2:0xFF,  3:0xFF,  4:0xFF,  5:0xFF,
6:0xFF,  7:0xFF

A24 Assign Base: 0x200000         A32 Assign Base:
0x20000000

DC Starting LA : 0x01,  BNO=YES   For FAILED Dev : DO
set Reset Bit

Servant Area   : 0x00             GPIB Primary   :
0x01

GPIB Addr Assgn: Default          GPIB Flags     :
MultSecond NAT4882 DMA

GPIB Addr Avoid: 0x00000000

<more>        CI Block Base  : 0x080000         CI
Num Blocks  : 0x00

------ Resident Code Instrument Locations ------

0x00: 00000000            0x01: 00000000
0x02: 00000000

0x03: 00000000            0x04: 00000000
0x05: 00000000

0x06: 00000000            0x07: 00000000
0x08: 00000000

0x09: 00000000            0x0A: 00000000
0x0B: 00000000

---- CI Nonvolatile User Configuration Variables ----

0x00:00000000      0x01:00000000      0x02:00000000
   0x03:00000000

0x04:00000000      0x05:00000000      0x06:00000000
   0x07:00000000

0x08:00000000      0x09:00000000      0x0A:00000000
   0x0B:00000000

0x0C:00000000      0x0D:00000000     0x0E:00000000
  0x0F:00000000
```


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```
0x10:00000000      0x11:00000000      0x12:00000000
   0x13:00000000

0x14:00000000      0x15:00000000      0x16:00000000
   0x17:00000000

0x18:00000000      0x19:00000000      0x1A:00000000
   0x1B:00000000

0x1C:00000000      0x1D:00000000      0x1E:00000000
   0x1F:00000000

  <<Press A Key to Return to Main Menu>>
```

8. Press the space bar and the following information should appear on the screen.

```
GPIB–VXI Nonvolatile Configuration Main Menu

                (C) 1995  National Instruments

     ================================================

   1). Read In Nonvolatile Configuration

   2). Print Configuration Information

   3). Change Configuration Information

   4). Set Configuration to Factory Settings

   5). Write Back (Save) Changes

   6). Quit Configuration

   Choice (1–6):
```

9. Enter a 3 and press return. The following information should appear on the screen.

```
GPIB–VXI Nonvolatile Configuration Changer

               (C) 1995 National Instruments


   0). Edit Local Register Configuration

   1). Edit pSOS Configuration

   2). Edit VXI Interrupt Handler Logical Addresses

   3). Edit Resource Manager Configuration

   4). Edit Servant Area and DC Configuration
```


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```
   5). Edit FAILED Device Handling Mode

   6). Edit GPIB Configuration

   7). Edit Default CI Configuration

   8). Edit Resident CI Base Locations

   9). Edit CI User Configuration Variables

   Q). Quit Editor

   Choice (0–9,Q):
```

10. Enter a 3 and press return. The following information should appear on the screen.

```
----- Resource Manager Configuration -----

Seconds to wait before starting Resource Manager
(default 0x0000):
```

11. Enter a 5 and press return. The following information should appear on the screen.

```
A24 Base Address to Start Assigning Memory Map (de-
fault 0x200000):
```

12. Press return. The following information should appear on the screen.

```
A32 Base Address to Start Assigning Memory Map (de-
fault 0x20000000):
```

13. Press return. The following information should appear on the screen.

```
 <<Press A Key to Return to Main Menu>>
```

14. Press the space bar and the following information should appear on the screen.

```
GPIB–VXI Nonvolatile Configuration Changer

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================================================

   0). Edit Local Register Configuration

   1). Edit pSOS Configuration

   2). Edit VXI Interrupt Handler Logical Addresses

   3). Edit Resource Manager Configuration
```


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```
   4). Edit Servant Area and DC Configuration
   5). Edit FAILED Device Handling Mode
   6). Edit GPIB Configuration
   7). Edit Default CI Configuration
   8). Edit Resident CI Base Locations
   9). Edit CI User Configuration Variables
   Q). Quit Editor
   Choice (0–9,Q):
```

15. Enter a Q and press return. The following information should appear on the screen.

```
GPIB–VXI Nonvolatile Configuration Main Menu
          (C) 1995  National Instruments
     ================================================
   1). Read In Nonvolatile Configuration
   2). Print Configuration Information
   3). Change Configuration Information
   4). Set Configuration to Factory Settings
   5). Write Back (Save) Changes
   6). Quit Configuration
   Choice (1–6):
```

16. Enter a 5 and press return. The following information should appear on the screen.

```
Saving Nonvolatile Configuration Information.
   Will take 5–10 seconds, Please wait.....Done!
<<Press A Key to Return to Main Menu>>
```

17. Press the space bar. The following information should appear on the screen.

```
GPIB–VXI Nonvolatile Configuration Main Menu
          (C) 1995  National Instruments
     ================================================
```


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```
1). Read In Nonvolatile Configuration

2). Print Configuration Information

3). Change Configuration Information

4). Set Configuration to Factory Settings

5). Write Back (Save) Changes

6). Quit Configuration

Choice (1–6):
```

18. Enter a 6 and press return. The following information should appear on the screen.

```
Must Re–Initialize pROBE or re–boot for pSOS changes
to take effect.

Other changes made automatically when configuration
saved.

*****************************************

*         DONE WITH CONFIGURATION        *

* Change Startup mode Settings to enter    *

* different mode or push RESET to re–boot. *

*****************************************
```

19. Power off the card cage and remove the RS-232 cable from the GPIB-VXI/C Slot 0. This completes the resource manager delay change.

If you need any assistance call 1-800-TEK-WIDE or contact your local Tektronix representative.

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